Qucs

Report Book
Technical reports and descriptions

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1 Verilog-AMS interface

1.1 Introduction
Verilog-AMS is a hardware description language. It can be used to specify the analogue behaviour of compact device models. Usually these are C or C++ implementations in analogue simulators. The effort to implement modern compact models in C/C++ is quite high compared to the description in Verilog-AMS.

1.2 ADMS
The software ADMS (see http://mot-adms.sourceforge.net) allows Verilog-AMS descriptions to be translated into any other programming language. It generates a structured XML tree representing the compact device model description.

![Diagram of ADMS data flow]

The internal XML tree is used to generate ready-to-compile C or C++ code which is specific to the simulators API. The code generator is able to produce

- evaluation of device equations (current and charge) including their derivatives,
• glue code for the simulator API,
• documentation and
• any other data described by the original Verilog-AMS input file.

1.3 XML admst scripts

The language transformation uses a language named admst. It is itself a XML description. The command line in order to run a transformation is

```
$ admsXml <device.va> -e <interface-1.xml> -e <interface-2.xml>
```

From version 0.0.11 Qucs comes with the following Verilog-AMS transformers

• `qucsMODULEcore.xml`
  creating the actual analogue simulator implementation

• `qucsMODULEdefs.xml`
  creating the parameter descriptions for the analogue simulator

• `qucsMODULEgui.xml`
  creating the implementation for the GUI integration

• `qucsVersion.xml`
  basic admst library

• `analogfunction.xml`
  creating analogue function code

In order to create admst scripts for a simulator it is necessary to understand both, the simulator specific API and how the ADMS data tree items – which are based on the Verilog-AMS source file describing the model – relate to the API.

The command lines for transforming a Verilog-AMS source file into the appropriate Qucs C++ source files are

```
$ admsXml <device.va> -e qucsVersion.xml -e qucsMODULEcore.xml
$ admsXml <device.va> -e qucsVersion.xml -e qucsMODULEgui.xml
$ admsXml <device.va> -e qucsVersion.xml -e qucsMODULEdefs.xml
$ admsXml <device.va> -e analogfunction.xml
```

each creating an appropriate *.cpp and *.h file.

The admst language is used to traverse the internal tree. The tree’s root is defined by the Verilog-AMS module definition.
module device (node1, node2, ...)
    // module definitions and code
endmodule

1.3.1 Short introduction into the admst language syntax

Usually the admst language instructions are basically formed as

\[
<\text{admst:instruction} \ \text{argument}=\ldots> \\
\ldots \\
</\text{admst:instruction}>
\]

or

\[
<\text{admst:instruction} \ \text{argument}=\ldots/> \\
\]

Any other text outside these instruction is output to the console or into an appropriate file. Some of the most important language construct are listed below.

- Traversing a list: The construct allows to traverse all children of the selected branch.

\[
<\text{admst:for-each} \ \text{select}="/\text{module}"> \\
\ldots \\
</\text{admst:for-each}>
\]

- Defining and using variables: Values from the data tree can be put into named and typed variables which are then accessible using the $ operator.

\[
<\text{admst:value-of} \ \text{select}="/\text{name}"> \\
<\text{admst:variable} \ \text{name}="/\text{module}" \ \text{select}="/\text{module}"> \\
\]

- Opening a file: Printed text (see below) is output into the given file.

\[
<\text{admst:open} \ \text{file}="/\text{module}.cpp"> \\
\ldots \\
</\text{admst:open}>
\]

- Output text: Special characters must be encoded (e.g. " \rightarrow \text{"}; \ \text{<} \rightarrow \text{&lt;}; \ \text{>} \rightarrow \text{&gt;} \ \text{and} \ \text{
} \rightarrow \text{\n}).

\[
<\text{admst:text} \ \text{format}="/\text{This is a text ./}> \\
\]

- Definition of a function: Functions in admst are called templates.
1.3.2 Analogue simulator script

The analogue simulator implementation consists of several parts. For each type of simulation appropriate functions must be implemented.

- DC simulation
  module::initDC (void),
  module::restartDC (void) and
  module::calcDC (void)

- AC simulation
  module::initAC (void) and
  module::calcAC (nr_double_t)

- S-parameter simulation
  module::initSP (void) and
  module::calcSP (nr_double_t)

- Transient simulation
  module::initTR (void) and
  module::calcTR (nr_double_t)

- AC noise simulation
  module::initNoiseAC (void) and
  module::calcNoiseAC (nr_double_t)

- S-parameter noise simulation
  module::initNoiseSP (void) and
  module::calcNoiseSP (nr_double_t)
Harmonic simulation

module::initHB (int) and
module::calcHB (int)

These functions go into the module.core.cpp file. An appropriate module.core.h header file is also created.

In case the Verilog-AMS source file contains analog functions in the module definition, e.g.

```
analog function real name;
    input x;
    real x;
    begin
        name = x * x;
    end
endfunction
```

the analogfunction.xml script produces the appropriate C/C++ and header files

- module.analogfunction.cpp
- module.analogfunction.h

The ADMS language transformer is aware of how analogue simulators solve a network of linear and non-linear devices. The general Newton-Raphson algorithm for a DC simulation used in SPICE-like simulators as well as in Qucs can be expressed as

\[
J^{(m)} \cdot V^{(m+1)} = J^{(m)} \cdot V^{(m)} - f\left(V^{(m)}\right) \\
= I_{lin}^{(m)} + I_{nl}^{(m)} - J_{nl}^{(m)} \cdot V^{(m)}
\]  

(1.1)

whereas \( J \) denotes the Jacobian

\[
J^{(m)} = \frac{\partial f (V)}{\partial V} \bigg|_{V^{(m)}}
\]  

(1.2)

There are basically two types of contributions supported by ADMS: currents and charges. The appropriate Jacobian matrices are

\[
J^{(m)} = J_I^{(m)} + J_Q^{(m)} = \underbrace{\frac{\partial I (V)}{\partial V}}_{\text{"static"}} \bigg|_{V^{(m)}} + \underbrace{\frac{\partial Q (V)}{\partial V}}_{\text{"dynamic"}} \bigg|_{V^{(m)}} = G + C
\]  

(1.3)

consisting of two real valued matrices \( G \) (conductance/transconductance matrix) and \( C \) (capacitance/transcapacitance matrix).
In the Verilog-AMS descriptions only the current and charge contributions are mentioned. The appropriate derivatives are meant to be automatically formed by the language translator ADMS.

\[
\begin{align*}
I(c_i, e_i) &\leftarrow i_t; \quad // \text{current contribution} \\
I(s_i, c_i) &\leftarrow ddt(Qjs); \quad // \text{charge contribution}
\end{align*}
\]

The right-hand side of eq. (1.1) consists of the linear and non-linear currents of the network as well as the Jacobian matrix multiplied by the voltage vector. Since devices are usually uncorrelated both parts can be computed directly on a per device basis.

### 1.3.3 Current limitations of ADMS

The following section contains some simple examples demonstrating which Verilog-AMS statements can be successfully handled by ADMS and which not.

**Example 1**

There was a bug in the `admst` scripts. They failed to place the function calls of analogue functions correctly. This has been fixed.

```verilog
module diode (a, c);
  inout a, c;
  electrical a, c;

  analog function real current;
    input is, v;
    begin
      current = is * (exp(v / 26e−3) − 1);
    end
  endfunction

  real Vd;
  real Id;

  analog begin
    Vd = V(a, c);
    Id = current (1e−15, Vd);
    I(a, c) <+ Id;
  end

endmodule
```

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Example 2

It is not allowed to mix current and charge contributions in assignments. Mixing both emits wrong C/C++ code. It accounts the current to be a charge in this case.

```plaintext
module diode(a, c);
  inout a, c;
  electrical a, c;

  real Vd, Id, Is, Cp;

  analog begin
    Is = 1e-15;
    Cp = 1e-12;
    Vd = V(a, c);
    Id = Is * (exp(Vd / 26e-3) - 1);

    // not allowed in ADMS
    I(a, c) <+ Id + ddt(Cp*V(a,c));

    // allowed in ADMS
    I(a, c) <+ Id;
    I(a, c) <+ ddt(Cp*V(a,c));
  end

endmodule
```

Example 3

The following example is rejected by the admst scripts with this error message.

```
[info] admst-2.2.4 Oct 18 2006 19:50:46
[fatal] qucsVersion.xml:1497:admst:if[lhs]: missing node source/insource
```

An immediate potential on the right hand side is not allowed embedded in a function.

```plaintext
module diode(a, c);
  inout a, c;
  electrical a, c;

  real Id, Is;
```
analog begin
    Is = 1e−15;
    Id = Is * (exp (V(a, c) / 26e−3) − 1);

    // not allowed in ADMS
    I(a, c) += Is * (exp (V(a, c) / 26e−3) − 1);

    // allowed in ADMS
    I(a, c) += Id;
end
endmodule

Example 4

Potentials on the left-hand side of contribution assignments are not allowed. This kind of assignment emits wrong C/C++ code.

module diode(a, c);
    inout a, c;
    electrical a, c;

    real Id, Is;
    real Rp;

    analog begin
        Rp = 1e9;
        Is = 1e−15;
        Id = Is * (exp (V(a, c) / 26e−3) − 1);
        I(a, c) += Id;

        // allowed in ADMS
        I(a, c) += V(a, c) / Rp;

        // not allowed in ADMS
        V(a, c) += I(a, c) * Rp;
end
endmodule
1.3.4 Code for the GUI integration

The **admst** script for the GUI creates files according to its API. Basically it produces the list of parameters as well their descriptions (if available) in a property list. Additionally the symbol drawing code is emitted which should be adapted to the devices requirements.

![Component property dialog in the GUI](image)

**Figure 1.2: component property dialog in the GUI**

In fig. 1.2 the component property dialog of an implemented device is shown. In the schematic in fig. 1.3 the symbol for the HICUM model is surrounded with a red circle. The GUI code is also responsible for the icons in the listview on the left hand side of the figure.
1.4 Adding Verilog-AMS devices to Qucs

The section gives an overview how to add a Verilog-AMS model to Qucs in a step-by-step manner. Be aware that the description is meant for advanced users partly familiar with the usual GNU/Linux build system and C/C++ programming.

1.4.1 The Verilog-AMS source file

The starting point of a new Verilog-AMS model in Qucs is the Verilog-AMS source file which must be aware of the discussed ADMS limitations. The example we are going to discuss is a simple diode model shown in the following listing contained in the `diode.va` file.

```plaintext
#include "disciplines.vams"
#include "constants.vams"

// ADMS specific definitions
```
module diode(a, c);
    // device terminals
    inout a, c;
    electrical a, c;

    // internal node
    electrical ci;

    // model parameters
    parameter real Is = 1E−15 from [0:1] 'attr(info="saturation_current");
    parameter real Cp = 1E−12 from [0:1] 'attr(info="parallel_capacitance");
    parameter real Rs = 1.0 from (0:inf) 'attr(info="series_resistance");
    parameter real Temp = 300 from (0:inf) 'attr(info="temperature");

    real Vd, Id, fourkt, twoq, Qp;

    analog begin
        Vd = V(a, ci);
        Id = Is * (exp (Vd / 26e−3) − 1);
        Qp = Cp * Vd;
        I(a, ci) <+ Id;
        I(a, ci) <+ ddt(Qp);
        I(ci, c) <+ V(ci, c) / Rs;

        begin : noise
            fourkt = 4.0 * 'P_K * Temp;
            twoq = 2.0 * 'P_Q;
            I(ci, c) <+ white_noise(fourkt/Rs, "thermal");
            I(a, ci) <+ white_noise(twoq*Id, "shot");
        end // noise
    end // analog
1.4.2 Integrating the model into the analogue simulator

The qucs-core tree of Qucs must be configured using the `--enable-maintainer-mode` option.

```
$ ./configure --enable-maintainer-mode --prefix=/tmp
```

The source trees of qucs (GUI) as well as qucs-core (simulator) are within the release tarballs available at [http://qucs.sourceforge.net/download.html](http://qucs.sourceforge.net/download.html). During development of new Verilog-A models it is recommended to use CVS. Latest CVS trees of qucs and qucs-core can be obtained using the following command lines.

```
$ cvs -z3 -d:pserver:anonymous@qucs.cvs.sourceforge.net:/cvsroot/qucs 
   co qucs-core
$ cvs -z3 -d:pserver:anonymous@qucs.cvs.sourceforge.net:/cvsroot/qucs 
   co qucs
```

Also the software `adms` must be installed. It is available at [http://sourceforge.net/projects/mot-adms](http://sourceforge.net/projects/mot-adms).

The file `diode.va` must be copied into the source tree.

```
$ cp diode.va qucs-core/src/components/verilog/
```

In this directory (`qucs-core/src/components/verilog/`) the Verilog model can be checked if it can be translated successfully using the following command lines.

```
$ admsXml diode.va -e qucsVersion.xml -e qucsMODULEcore.xml
[iinfo] admsXml-2.2.4 Oct 18 2006 19:50:46
[iinfo] diode.core.cpp and diode.core.h: files created
[iinfo] elapsed time: 0.0339946
[iinfo] admst iterations: 4146 (4146 freed)
$ admsXml diode.va -e analogfunction.xml
[iinfo] admsXml-2.2.4 Oct 18 2006 19:50:46
[iinfo] diode.analogfunction.h created
[iinfo] diode.analogfunction.cpp created
[iinfo] elapsed time: 0.0262961
[iinfo] admst iterations: 3919 (3919 freed)
```

These command lines create the files for the model evaluation code. The file names (`diode.*`) are due to the name of the module contained in the Verilog-AMS source file.

Additionally the source code must be changed in some more locations.
- **src/components/component.h**
  In this file it is necessary to add the line
  ```
  #include "verilog/diode.core.h"
  ```

- **src/components/component_id.h**
  The file contains unique component identifiers. It is necessary to add the
  Verilog modules name.
  ```
  enum circuit_type {
    CIR_UNKNOWN = -1,
    ...
    // verilog devices
    CIR_diode,
    ...
  };
  ```

- **src/input.cpp**
  In order to be able to instantiate the new model the file must be modified as
  follows.
  ```
  // The function creates components specified by the type of component.
  circuit * input::createCircuit (char * type) {
    if (!strcmp (type, "Pac"))
      return new pac ();
    ...
    else if (!strcmp (type, "diode"))
      return new diode ();

    logprint (LOG_ERROR, "no such circuit type '%s'
    type);
    return NULL;
  }
  ```

- **src/qucsdefs.h**
  Finally the properties including their range definitions must be added to this
  file. The appropriate file can be obtained using the following command line.
  ```
  $ admsXml diode.va -e qucsVersion.xml -e qucsMODULEdefs.xml
  [info] admsXml-2.2.4 Oct 18 2006 19:50:46
  [info] diode.defs.h: file created
  [info] elapsed time: 0.0335337
  [info] admst iterations: 4294 (4294 freed)
  ```
  The emitted file **diode.defs.h** looks like
  ```
  /* diode verilog device */
  { "diode", 2, PROP_COMPONENT, PROP_NO_SUBSTRATE, PROP_NONLINEAR,
    ```
representing the parameters defined in the original Verilog-AMS file. This excerpt must be included in the `src/qucsdefs.h` file into this structure:

```c
// List of available components.
struct define_t qucs_definition_available[] =
{
    .../* end of list */
    { NULL, 0, 0, 0, 0, { PROP_NO_PROP }, { PROP_NO_PROP } }
};
```

Finally the `Makefile.am` in the `src/components/verilog/` directory must be adjusted to make the build-system aware of the new component. There must be added:

```makefile
libverilog_a_SOURCES = ... \
    diode.analogfunction.cpp diode.core.cpp

noinst_HEADERS = ... \
    diode.analogfunction.h diode.core.h

VERILOG_FILES = ... diode.va

if MAINTAINER_MODE
...
diode.analogfunction.cpp: analogfunction.xml
        $(ADMSXML) $< -e analogfunction.xml
diode.core.cpp: qucsVersion.xml qcusMODULEcorexml
        $(ADMSXML) $< -e qucsVersion.xml -e qcusMODULEcorexml
diode.defs.h: qucsVersion.xml qcusMODULEdefs.xml
        $(ADMSXML) $< -e qucsVersion.xml -e qcusMODULEdefs.xml
diode.gui.cpp: qucsVersion.xml qcusMODULEgui.xml
        $(ADMSXML) $< -e qucsVersion.xml -e qcusMODULEgui.xml
```
in order to create the correct build rules.

If everything worked fine then the new Verilog-AMS model is now completely integrated into the analogue simulator.

### 1.4.3 Integrating the model into the GUI

Very likely as the qucs-core tree in the previous section also the qucs source tree must be configured using the --enable-maintainer-mode option.

```
$ ./configure --enable-maintainer-mode --prefix=/tmp
```

Still in the `qucs-core/src/components/verilog` directory it is now necessary to create the C++ code for the GUI using the following command line.

```
$ admsXml diode.va -e qucsVersion.xml -e qucsMODULEgui.xml
```

Both the created files `diode.gui.cpp` and `diode.gui.h` should be copied to the `qucs/qucs/components` directory.

Depending on the type of device several changes must be applied to these files. The constructor will basically contain the properties of the device as they are going to occur in the component property dialog as depicted in fig. 1.2. Check these if they are complete or if some can be left.

```cpp
diode::diode()
{
    Description = QObject::tr ("diode
    verilog
    device");

    Props.append (new Property ("Is", "1E-15", false,
        QObject::tr ("saturation
        current")));
    Props.append (new Property ("Cp", "1E-12", false,
        QObject::tr ("parallel
        capacitance")));
    Props.append (new Property ("Rs", "1.0", false,
        QObject::tr ("series
        resistance")));
    Props.append (new Property ("Temp", "300", false,
```
QObject::tr ("temperature");
...

The diode::info function should be adapted to meet the devices requirements. The BitmapFile should be changed to represent a correct PNG file in the qucs/bitmaps directory. Both the Name and the bitmap are going to appear in the left-hand component tab as shown in fig. 1.3.

    Element * diode::info (QString& Name, char * &BitmapFile, bool getNewOne)
    {
        Name = QObject::tr ("Diode");
        BitmapFile = "diode";
        if (getNewOne) return new diode();
        return 0;
    }

The diode::info_pnp() method can be completely deleted. It can be necessary for bipolar transistors where two types of devices could be displayed (npn and pnp type). The method must also be deleted from the header file. Also, in this case, the new diode class inherits Component instead of MultiViewComponent.

The diode::createSymbol() method must be adapted to represent a valid schematic symbol. Anyway, the default code can be used as a template.

    void diode::createSymbol()
    {
        // normal bipolar
        Lines.append (new Line (−10,−15,−10, 15,QPen(QPen::darkBlue ,3)));
        Lines.append (new Line (−30, 0,−10, 0,QPen(QPen::darkBlue ,2)));
        Lines.append (new Line (−10, −5, 0,−15,QPen(QPen::darkBlue ,2)));
        Lines.append (new Line ( 0,−15, 0,−30,QPen(QPen::darkBlue ,2)));
        Lines.append (new Line (−10, 5, 0, 15,QPen(QPen::darkBlue ,2)));
        Lines.append (new Line ( 0, 15, 0, 30,QPen(QPen::darkBlue ,2)));

        // substrate node
        Lines.append (new Line ( 9, 0, 30, 0,QPen(QPen::darkBlue ,2)));
        Lines.append (new Line ( 9, −7, 9, 7,QPen(QPen::darkBlue ,3)));

        // thermal node
        Lines.append (new Line (−30, 20,−20, 20,QPen(QPen::darkBlue ,2)));
        Lines.append (new Line (−20, 17,−20, 23,QPen(QPen::darkBlue ,2)));
        //
if (Props.getFirst()->Value == "npu") {
    Lines.append(new Line(-6, 15, 0, 15, QPen(QPen::darkBlue, 2)));
    Lines.append(new Line(0, 9, 0, 15, QPen(QPen::darkBlue, 2)));
} else {
    Lines.append(new Line(-5, 10, -5, 16, QPen(QPen::darkBlue, 2)));
    Lines.append(new Line(-5, 10, 1, 10, QPen(QPen::darkBlue, 2)));
}

// terminal definitions
Ports.append(new Port(0, -30)); // collector
Ports.append(new Port(-30, 0)); // base
Ports.append(new Port(0, 30)); // emitter
Ports.append(new Port(30, 0)); // substrate
Ports.append(new Port(-30, 20)); // thermal node

// relative bounding
x1 = -30; y1 = -30;
x2 = 30; y2 = 30;

In order to test the component in the GUI it is necessary to modify some more source code files.

- **qucs/qucs.cpp**
  In this file the new Verilog device will be made available to the component tab. If a new non-linear device is added then place it here:
  ```cpp
  pInfoFunc nonlinearComps[] =
  { ... &diode::info, 0};
  ```

- **qucs/components/component.cpp**
  The new verilog device must be loadable in the GUI. So in the function `getComponentFromName()` add this:
  ```cpp
  Component* getComponentFromName(QString& Line)
  {
      ...
      case 'd' : if(cstr == "iode") c = new diode();
                  break;
      ...
      return c;
  }
  ```

- **qucs/components/components.h**
  In the component header file it is necessary to add:
#include "diode.h"

In order to make the build-system aware of the new Verilog model the file `qucs/components/Makefile.am` must be modified in the following way.

libcomponents_a_SOURCES = ... \
    diode.gui.cpp

noinst_HEADERS = ... \
    diode.gui.h

With these steps the component is now fully integrated into the GUI.

## 1.5 Implemented devices

The following sections presents the models already added in Qucs including some test schematics and simulation results.

### 1.5.1 HICUM/L2 v2.11 model

The name HICUM was derived from HIgh-CUrrent Model, indicating that HICUM initially was developed with special emphasis on modelling the operating region at high current densities which is very important for certain high-speed applications.

The Verilog-AMS source code can be obtained from [http://www.iee.et.tu-dresden.de/iee/eb/hic_new/hic_source.html](http://www.iee.et.tu-dresden.de/iee/eb/hic_new/hic_source.html). The model used in Qucs was a bit modified due to some ADMS limitations.

Some schematics have been setup to verify that the model emits basically the correct output values and the source code translations worked properly.

**DC simulation**

The setup for the forward Gummel plot is depicted in fig. 1.4. The base-emitter voltage is swept ($V_{BE} = 0.2 \ldots 1.2$) with a constant voltage across the second diode $V_{BC} = 0$. 

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Figure 1.4: forward Gummel plot schematic for HICUM/L2 v2.11 model

In fig. 1.5 the logarithmic Gummel plot is shown including the ratio between the base current and collector current on the secondary axis.
Figure 1.5: forward Gummel plot for HICUM/L2 v2.11 model

DC simulation

In fig. 1.6 the schematic for the output characteristics of the HICUM model is shown. The 2-dimensional sweep describes the function

$$I_C = f(V_{CE}, V_{BE})$$

(1.4)
Figure 1.6: output characteristics schematic for HICUM/L2 v2.11 model

Figure 1.7 shows the results of the DC simulations for the output characteristics of the bipolar transistor.
Figure 1.7: output characteristics plot for HICUM/L2 v2.11 model

**AC simulation**

Figures 1.8 and 1.9 depict the schematic and diagrams for an AC simulation in a given bias point. The current gains magnitude and phase are shown as well as the characteristics of the small signal base and collector current in the complex plane (polar plot).
Figure 1.8: AC simulation schematic for HICUM/L2 v2.11 model

Figure 1.9: AC simulation plot for HICUM/L2 v2.11 model
S-parameter simulation

In the figures 1.10 and 1.11 a two-port S-parameter simulation schematic (including noise) as well as the results are shown. The four S-parameters are displayed in two Polar-Smith combi diagrams. The noise figure as well as the minimal noise figure are displayed in a logarithmic Cartesian diagram.

Figure 1.10: S-parameter simulation schematic for HICUM/L2 v2.11 model
Figure 1.11: S-parameter simulation plot for HICUM/L2 v2.11 model

**Transient simulation**

In the schematic in fig. 1.12 a current pulse is fed into the base of the transistor. Varying the input capacitance changes the response in the collector current as shown in fig. 1.13.
Figure 1.12: Transient simulation schematic for HICUM/L2 v2.11 model

Figure 1.13: Transient simulation plot for HICUM/L2 v2.11 model
1.5.2 FBH-HBT model version 2.1

The HBT (Hetero Bipolar Transistor) model developed by Matthias Rudolph at the FBH (Ferdinand-Braun-Institut für Hochfrequenztechnik) is available in the Internet at http://www.designers-guide.org/VerilogAMS.

DC simulation

Forward Gummel plot.

![Forward Gummel plot schematic for HBT model](image)

Figure 1.14: forward Gummel plot schematic for HBT model

DC simulation

Output characteristics.
1.6 End Note

The preferred way to add a new Verilog model to Qucs is certainly to prepare a model, check if it is accepted by ADMS and finally ask the maintainers to integrate it. Until there is no possibility to load device modules dynamically (which is on the TODO list) too many hand-made changes have to be done to automate this process. The dynamic modules require changes in the simulator API as well in the GUI code.

Furthermore work is going to be continued on ADMS itself as well as on the admst scripts.

The authors would like to thank Hélène Parruitté for the initial implementation of the Verilog-AMS interface in Qucs. Also thanks go to the company Xmod Technologies (see http://www.xmodtech.com) allowing her to work on such an interface and finally to share the outcome of her internship under the GPL.
2 Verilog-A Modular Macromodel for Operational Amplifiers

2.1 Introduction

Since the release of Qucs version 0.0.11 the Qucs team has spent a lot of time and effort improving and debugging the Qucs device and circuit modelling facilities. Initially, the primary device and circuit modelling technique available to users was based on a subcircuit approach that allowed new models to be formed from the built in components distributed with each release of the package\(^1\). Releases 0.0.11 and 0.0.12 added model construction centred around the nonlinear equation defined device (EDD) and ADMS compact device models. For these modelling techniques preliminary documentation and application information has been posted on the Qucs Web site\(^2\), outlining the fundamental basis of these procedures. Unfortunately, both the EDD and ADMS modelling techniques do require a level of specialised knowledge which many Qucs users may be unfamiliar with. These notes have been written in the hope that the information they provide will help add to the body of information published on Qucs modelling and also be useful to other Qucs users who would like to try constructing, and experimenting with, new device and circuit models using the ADMS software. Today Qucs has moved on from simply a GPL circuit simulator with user friendly schematic capture, and has started to evolve into an advanced circuit and device modelling tool which offers features that were not commonly available in previous generations of GPL circuit simulators. This report introduces an ADMS synthesised compact macromodel for the modular operational amplifier previously described

\(^1\)It is also possible to construct models directly in C++ and compile and link them to the main body of the Qucs code. This is the approach taken by the package developers. However, for the average Qucs user who is primarily interested in using the package, rather than taking part in it’s development, this route to model development is not really an option.

in the Qucs tutorial on operational amplifiers.\textsuperscript{3} This macromodel is characterised by a similar symbol to the primitive operational amplifier gain block included with all Qucs releases. However, it provides Qucs with a more realistic general purpose operational amplifier model that can be used with confidence when designing many practical circuits which are dependent on amplifier characteristics for correct operation. The process of compiling and linking ADMS generated C++ models with the Qucs C++ code has been a learning vehicle on my part, allowing some of the complexities of the ADMS Verilog-A compiler to be decoded and understood. The ADMS synthesised operational amplifier macromodel also marks a departure from the previously described Qucs compact device models in that it represents a circuit function rather than a semiconductor device characteristic. The source code for the modular macromodel is included in this report and the ADMS generated C++ code can be found in the Qucs release source tarballs archive\textsuperscript{4}. The procedure used to synthesize and link the model to Qucs followed the route suggested by Stefan and Hélène in their report on the Verilog-AMS/Qucs interface.

2.2 A Modular Macromodel for an Operational Amplifier

An introduction to the technical specification and structure of a modular macromodel for a general purpose operational amplifier is given on page 7 of the Qucs operational amplifier tutorial. The characteristics of this operational amplifier macromodel are:

- Input stage: Offset voltage and current, bias current, differential resistance and capacitance.
- Gain stages: Two pole differential response and single zero common-mode response.
- Large signal response: Slew rate limiting.
- Output stage: Resistance, output voltage and current limiting.

2.3 Parameters

\textsuperscript{3}Mike Brinson, “Qucs Tutorial: Modelling Operational Amplifiers”, http://qucs.sourceforge.net/docs.html.
\textsuperscript{4}Available from http://qucs.sourceforge.net/download.html
<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>GBP</td>
<td>GBP</td>
<td>Gain bandwidth product</td>
<td>Hz</td>
<td>1e6</td>
</tr>
<tr>
<td>AOLDC</td>
<td>AOLDC</td>
<td>Open-loop differential gain at DC</td>
<td>dB</td>
<td>106.0</td>
</tr>
<tr>
<td>FP2</td>
<td>FP2</td>
<td>Second pole frequency</td>
<td>Hz</td>
<td>3e6</td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>Output resistance</td>
<td>Ω</td>
<td>75</td>
</tr>
<tr>
<td>CD</td>
<td>CD</td>
<td>Differential input capacitance</td>
<td>F</td>
<td>1e-12</td>
</tr>
<tr>
<td>RD</td>
<td>RD</td>
<td>Differential input resistance</td>
<td>Ω</td>
<td>2e6</td>
</tr>
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<td>IOFF</td>
<td>IOFF</td>
<td>Input offset current</td>
<td>A</td>
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<tr>
<td>IB</td>
<td>IB</td>
<td>Input bias current</td>
<td>A</td>
<td>80e-9</td>
</tr>
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<td>VOFF</td>
<td>Input offset voltage</td>
<td>V</td>
<td>7e-4</td>
</tr>
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<td>CMRRDC</td>
<td>CMRRDC</td>
<td>Common-mode rejection ratio at DC</td>
<td>dB</td>
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<tr>
<td>FCM</td>
<td>FCM</td>
<td>Common-mode zero corner frequency</td>
<td>Hz</td>
<td>200.0</td>
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<tr>
<td>PSRT</td>
<td>PSRT</td>
<td>Positive slew rate</td>
<td>V/s</td>
<td>5e5</td>
</tr>
<tr>
<td>NSRT</td>
<td>NSRT</td>
<td>Negative slew rate</td>
<td>V/s</td>
<td>5e5</td>
</tr>
<tr>
<td>VLIMP</td>
<td>VLIMP</td>
<td>Positive output voltage limit</td>
<td>V</td>
<td>14</td>
</tr>
<tr>
<td>VLIMN</td>
<td>VLIMN</td>
<td>Negative output voltage limit</td>
<td>V</td>
<td>-14</td>
</tr>
<tr>
<td>ILMAX</td>
<td>ILMAX</td>
<td>Maximum output current at DC</td>
<td>A</td>
<td>35e-3</td>
</tr>
<tr>
<td>CSCALE</td>
<td>CSCALE</td>
<td>Current limit scale factor</td>
<td></td>
<td>50</td>
</tr>
</tbody>
</table>

* The default parameters are for a typical UA741 Operational Amplifier.

### 2.4 Verilog-A model code

```verilog
// Qucs modular OP AMP model:
// Default parameters are for a typical UA741.
//
// This is free software; you can redistribute it and/or modify
// it under the terms of the GNU General Public License as published by
// the Free Software Foundation; either version 2, or (at your option)
// any later version.
//
// Copyright (C), Mike Brinson, mbrin72043@yahoo.co.uk, November 2007.
//
'include "disciplines.vams"
'include "constants.vams"

module mod_amp ( in_p, in_n, out_p );
inout in_p, in_n, out_p;
electrical in_p, in_n, out_p;
electrical n2, n3, n4, n5, n6, n7, n8, n9, n10, n11, n12;

'define attr(txt) (*txt*)

parameter real GBP =1e6 from [1 : inf]
  "attr(info="Gain\_bandwidth\_product\(\text{Hz}\)\")
parameter real AOLDC = 106.0 from [0.01 : inf]
  "attr(info="Open\_loop\_DC\_gain\(\text{dB}\)\")
parameter real FP2 = 3e6 from [0.01 : inf]
  "attr(info="Second\_pole\_frequency\(\text{Hz}\)\")
```
parameter real RO = 75 from [0.01 : inf]
  'attr (info="Output resistance (Ohm)");
parameter real CD = 1e-12 from [1e-20 : inf]
  'attr (info="Differential input capacitance (F)");
parameter real RD = 2e6 from [0.01 : inf]
  'attr (info="Differential input resistance (Ohm)");
parameter real IOFF = 20e-9 from [1e-20 : inf]
  'attr (info="Input offset current (A)");
parameter real IB = 80e-9 from [1e-20 : inf]
  'attr (info="Input bias current (A)");
parameter real VOFF = 7e-4 from [0 : inf]
  'attr (info="Common mode rejection ratio at DC (dB)");
parameter real FC = 200 from [0.01 : inf]
  'attr (info="Common mode zero corner frequency (Hz)");
parameter real PSRT = 5e5 from [1 : inf]
  'attr (info="Positive slew rate (V/s)’");
parameter real NSRT = 5e5 from [1 : inf]
  'attr (info="Negative slew rate (V/s)’");
parameter real VLIMP = 14 from [0.01 : inf]
  'attr (info="Positive output voltage limit (V)’");
parameter real VLMN = -14 from [-inf : 0]
  'attr (info="Negative output voltage limit (V)’");
parameter real ILMAX = 35e-3 from [1e-9 : inf]
  'attr (info="Maximum DC output current (A)");
parameter real SCALE = 50 from [0 : inf]
  'attr (info="Current limit scaling factor");

real RP1, CP1, RP2, CP2;
real Rdiff, Voffset;
real CMRR0, CMgain, CM;
real Slewratapositive, Slewratangentative;
real MTWOP1;

//
// Constants
//
MTWOP1 = 6.28318530717958647693;

// Design equations
//
Voffset = VOFF*5;
Rdiff = RD/2;
CMRR0 = pow(10, CMRRDC/20);
CMgain = 1e6/CMRR0;
CM = 1.0/(MTWOP1*1e6*FC);
RP1 = pow(10, AOLDC/20);
CP1 = 1/(MTWOP1*GBP);
RP2 = 1;
CP2 = 1/(MTWOP1*FP2);
Slewratapositive = PSRT/(MTWOP1*GBP);
Slewratangentative = NSRT/(MTWOP1*GBP);

// Input voltage offset

I(in_p, n7) += V(in_p, n7);
I(in_p, n7) += Voffset;

I(in_a, n9) += V(in_a, n9);
I(in_a, n9) += -Voffset;
// Input bias currents
I(n7) <+ IB;
I(n9) <+ IB;

// Input current offset
I(n7, n9) <+ IOFF/2;

// Input differential resistance and capacitance
I(n7, n8) <+ V(n7, n8)/Rdiff;
I(n9, n8) <+ V(n9, n8)/Rdiff;
I(n7, n9) <+ ddt(CD∗V(n7, n9));

// Common mode stage
I(n6) <+ −CMgain∗V(n8);
I(n6) <+ V(n6);
I(n6, n10) <+ V(n6, n10)/1e6;
I(n6, n10) <+ ddt(CCM∗V(n6, n10));
I(n10) <+ V(n10);

// Differential mode and common mode signal adder stage
I(n11) <+ −V(n10);
I(n11) <+ −V(n7, n9);
I(n11) <+ V(n11);

// Slew rate limiting stage
if (V(n11) > Slewratepositive) I(n12) <+ −Slewratepositive;
else if (V(n11) < −Slewratenegative) I(n12) <+ Slewratenegative;
else I(n12) <+ −V(n11);
I(n12) <+ V(n12);

// First pole
I(n3) <+ −V(n12);
I(n3) <+ V(n3)/RP1;
I(n3) <+ ddt(CP1∗V(n3));

// Second pole
I(n5) <+ −V(n3);
I(n5) <+ V(n5)/RP2;
I(n5) <+ ddt(CP2∗V(n5));

// Current limiter stage
if (V(n2, out_p) >= ILMAX) begin
  I(n4) <+ −V(n5);
  I(n4) <+ CSCALE∗V(n5)*(V(n2, out_p) − ILMAX);
  I(n4) <+ V(n4);
end
else if (V(n2, out_p) <= −ILMAX) begin
  I(n4) <+ −ILMAX;
end
I (n4) <= -V(n5);
I (n4) <= -CSCALE*V(n5)*(V(n2, out_p) + ILMAX);
I (n4) <= V(n4);
end
else
begin
I (n4) <= -V(n5);
I (n4) <= V(n4);
end
// Output resistance
//
I(n4, n2) <= V(n4, n2)/(RO-1);
I(n2, out_p) <= V(n2, out_p);
//
// Voltage limiter stage
//
if (V(out_p) > VLIMP)
begin
I(out_p) <= -10.0*VLIMP;
I(out_p) <= 10.0*V(out_p);
end
else if (V(out_p) < VLIMN)
begin
I(out_p) <= -10.0*VLIMN;
I(out_p) <= 10.0*V(out_p);
end
end
endmodule

The ADMS syntax is a subset of Verilog-A. Allowed language structures are outlined in a SYNTAX-SUPPORTED file which can be downloaded from http://mot-adms.sourceforge.net.

2.5 Model test examples

In the following sections a series of test results are presented. These illustrate how the modular macromodel performs in comparison to the transistor level\(^5\) model for the UA741 operational amplifier. Typical parameters for the UA741 operational amplifier are listed in the introduction to this report. These values have been extracted from UA741 device data sheets provided by manufacturers. In the test simulations the modular UA741 parameters have been adjusted to give similar simulation results obtained from the transistor level model. A number of interesting differences between the simulation results obtained with the modular macromodel, plus default parameters, and the transistor level model are observed, for example the transistor level simulation results yield a value for IOFF of approximately zero amperes. With a real device this is unlikely to occur due to mismatches in the input transistor properties. In the transistor level model the input transistors are identical implying perfect matching. This is, of course, unlikely to be the case

\(^5\)The UA741 transistor level model can be found in the Qucs OpAmps component library.
with a real device. Once again the results demonstrate one of the most important rules in circuit simulation, namely that the accuracy of the results from a specific simulation does largely depend on how well a model represents a physical device or circuit. Further comments about the Verilog-A code and the accuracy of the simulation results are given with each set of test results.

2.5.1 Input voltage offset

Input voltage offset is represented by the Verilog-A code listed in this section. This models the input voltage offset by two batteries of value $V_{OFF}/2$. These are formed by current generators in parallel with one Ohm resistors. Notice that the direction of the current generator current flow determines the polarity of the batteries.

```verilog
// Input voltage offset
//
I(inp, n7) <+ V(inp, n7);
I(inp, n7) <+ Voffset;

I(in, n9) <+ V(in, n9);
I(in, n9) <+ -Voffset;
```

![Figure 2.1: UA741 modular macromodel input voltage offset test circuit and results](image)

Figure 2.1: UA741 modular macromodel input voltage offset test circuit and results
2.6 Input bias and offset currents

Input bias and offset currents are represented by the Verilog-A code listed in this section. Simple current generators are employed to model the input current effects. Values for IB and IOFF can be extracted from the results given in Figs. 2.3 and 2.4, using equations (2.1) and (2.2).

\[
V_p = - \left( IB + \frac{IOFF}{2} \right) \cdot 1e3
\]  

\[
V_n - V_s = \left( \frac{IOFF}{2} - IB \right) \cdot 1e3
\]  

The remainder of the input stage Verilog-A code adds differential input resistance and capacitance to the input stage of the operational amplifier macromodel.

```verilog-a
// Input bias currents
//
I(n7) <+ IB;
I(n9) <+ IB;

// Input current offset
//
I(n7, n9) <+ IOFF/2;

// Input differential resistance and capacitance
//
I(n7, n8) <+ V(n7, n8)/Rdiff;
I(n9, n8) <+ V(n9, n8)/Rdiff;
I(n7, n9) <+ ddt(CD*V(n7, n9));
```

Figure 2.2: UA741 transistor level input voltage offset test circuit and simulation results
Figure 2.3: UA741 modular macromodel input bias and offset current test circuit and simulation results
Figure 2.4: UA741 transistor level input bias and offset current test circuit and simulation results
2.7 Open loop differential voltage gain

Differential voltage gain is represented by the Verilog-A code listed in this section. Differential gain is modelled with three distinct quantities. These are 1. resistor RP1 which is set equal to the open loop differential gain at DC, 2. the primary pole in the voltage gain frequency response which is set by capacitor CP1, and 3. a high frequency pole set by CP2 and resistor RP2. Each pole stage is driven by a voltage controlled current generator. Note the current generator negative sign. This is required to maintain the correct signal phase. The derivation, and a more detailed discussion, of the model open-loop differential voltage gain properties can be found in pages 13 to 19 of the Qucs operational amplifier tutorial. Simulated results for the open-loop differential gain response are shown in Figs. 2.5 and 2.6. The AOLDC and CD parameters given in Fig. 2.5 have been adjusted to give the same response as the Qucs transistor level model. Again due to perfect transistor matching a value of CD roughly zero is required to produce similar high frequency responses above the second pole frequency.

```verbatim
// First pole
I(n3) <+ -V(n12);
I(n3) <+ V(n3)/RP1;
I(n3) <+ ddt(CP1*V(n3));
// Second pole
I(n5) <+ -V(n3);
I(n5) <+ V(n5)/RP2;
I(n5) <+ ddt(CP2*V(n5));
```


Figure 2.5: UA741 modular macromodel open-loop differential voltage gain test circuit and simulation results
Figure 2.6: UA741 transistor level open-loop differential voltage gain test circuit and simulation results
2.8 Common mode effects

Operational amplifier common-mode effects are represented by the Verilog-A code listed in this section. Common-mode effects are simulated using an identical network to that outlined in page 20 the Qucs operational amplifier tutorial. The simulated results for a unity gain CMMR test circuit are illustrated in Figs. 2.7 and 2.8. The macromodel parameters CMRR and FCM have been set at their default values to demonstrate the difference when compared to the transistor level model. Common-mode simulation results observed with the transistor level model are significantly better than those obtained from measurements on real devices, mainly because the simulation model is constructed from perfectly matched transistors. Associated with the differential amplifier stages and the common-mode section of the macromodel is a signal adder which combines the differential and common-mode signals. The Verilog code for this adder stage is also repeated with common-mode code. An adder can be formed by a one Ohm resistor driven by differential and common-mode currents. The resulting volt drop across the one Ohm resistor then becomes the sum of the two signal voltages.

```verbatim
// Common mode stage
//
I(n6) <+ -CMgain*V(n8);
I(n6) <+ V(n6);
I(n6, n10) <+ V(n6, n10)/1e6;
I(n6, n10) <+ ddt(CCM*V(n6, n10));
I(n10) <+ V(n10);
//
// Differential mode and common mode signal adder stage
//
I(n11) <+ -V(n10);
I(n11) <+ -V(n7, n9);
I(n11) <+ V(n11);
//
```
Figure 2.7: UA741 modular macromodel CMRR test circuit and simulation results

Figure 2.8: UA741 transistor level CMRR test circuit and simulation results
2.9 Slew rate limiting

Operational amplifier slew rate limiting effects are represented by the Verilog-A code listed in this section. Slew rate limiting can be modelled in Verilog-A using the if-else language statement. This allows the maximum signal current at node n12 to be limited to a value set by variables Slewratepositive or Slewratenegative which in turn are functions of parameters PSRT and NSRT (see page 25 of the Qucs operational amplifier tutorial). Again please note the sign of I(n12). The simulated results for a UA741 slewrate limiting test circuit are illustrated in Figs. 2.9 and 2.10. In general the results are very similar for both models. However, there is one point worth commenting on; in the case of the transistor level model there is a marked difference in the level of slewing for negative and positive signals (see waveform Vout3 in Fig. 2.10). This effect is probably due to the fact that the UA741 operational amplifier circuitry is very different near the power supply rails, resulting in significant differences in signal shape at high signal swings. This effect is not modelled by the modular macromodel.

```verbatim
// Slew rate limiting stage
//
if (V(n11) > Slewratepositive)
    I(n12) <+ -Slewratepositive;
else if (V(n11) < -Slewratenegative)
    I(n12) <+ Slewratenegative;
else I(n12) <+ -V(n11);
I(n12) <+ V(n12);
```
Figure 2.9: UA741 modular macromodel slewrate limiting test circuit and simulation results
Figure 2.10: UA741 transistor level slewrate limiting test circuit and simulation results
2.10 Output voltage limiting

Operational amplifier output voltage limiting effects are represented by the Verilog-A code listed in this section. A Verilog-A if-else statement is used to model voltage limiting. This language construction also demonstrates the use of the Verilog-A block construction formed with begin-end code words. Effectively the if-else statement swaps circuit elements as the voltage signal polarity changes. The simulated results for a UA741 voltage limiting test circuit are illustrated in Figs. 2.11 and 2.12. Again the results are very similar for both models. However, in the case of the macromodel there is no attempt to reduce the differential gain when output voltage limiting occurs and as a result some waveform distortion takes place. In practice if, as in the case of pure AC simulation, output voltage limiting is not required then simply set VLIMP and VLIMN well outside the range of required operating voltage and voltage limiting is never triggered.

```plaintext
// Voltage limiter stage
//
if (V(out_p) > VLIMP)
begin
    I(out_p) <+ -10.0*VLIMP;
    I(out_p) <+ 10.0*V(out_p);
end
else if (V(out_p) < VLIMN)
begin
    I(out_p) <+ -10.0*VLIMN;
    I(out_p) <+ 10.0*V(out_p);
end
end
```
Figure 2.11: UA741 modular macromodel output voltage limiting test circuit and simulation results
Figure 2.12: UA741 transistor level output voltage limiting test circuit and simulation results
2.11 Output current limiting

Operational amplifier output current limiting effects are represented by the Verilog-A code listed in this section. A Verilog-A if-else statement is used to model current limiting. The effect is modelled by a feedback mechanism which reduces the magnitude of current I(n4) which is proportional to the difference of the current flowing in the output path and ILMAX. A scale factor CSCALE is used to adjust maximum clamped output current. The simulated results for a UA741 current limiting test circuit are illustrated in Figs. 2.13 and 2.14. Current clamping induces distortion in the output waveform. Both the macromodel and the transistor level model give roughly the same clamped output currents but the wave shapes, and hence the distortion, are somewhat different. This is not surprising as the macromodel does not include a mechanism to control clamping distortion. Setting CSCALE to zero removes the current limiting process from the operational amplifier macromodel.

```
// Current limiter stage
//
if (V(n2, out_p) >= ILMAX)
begin
    I(n4) <+ -V(n5);
    I(n4) <+ CSCALE*V(n5)*(V(n2, out_p) - ILMAX);
    I(n4) <+ V(n4);
end
else if (V(n2, out_p) <= -ILMAX)
begin
    I(n4) <+ -V(n5);
    I(n4) <+ -CSCALE*V(n5)*(V(n2, out_p) + ILMAX);
    I(n4) <+ V(n4);
end
else
begin
    I(n4) <+ -V(n5);
    I(n4) <+ V(n4);
end
```
Figure 2.13: UA741 modular macromodel output current limiting test circuit and simulation results

Figure 2.14: UA741 transistor level output current limiting test circuit and simulation results
2.12 End note

These notes summarise a number of techniques for modelling operational amplifier functions using Verilog-A. Verilog-A is primarily intended for modelling compact semiconductor devices. However, as this report demonstrates it can be equally employed for macromodelling of integrated circuits and circuits in general. The Qucs C++ code for the modular operational amplifier model, generated by ADMS, can be found in the Qucs release source tarballs at http://qucs.sourceforge.net. The procedure followed to convert the Verilog-A code into C++ for compilation and linking with Qucs closely followed that described by Sefan Jahn and Hélène Parruitte. Although it takes more work to construct models using ADMS the effort is worthwhile because the finished models are very efficient in terms of memory usage and have significantly reduced run times. One interesting observation which is worth recording here is the fact that Qucs equation defined device (EDD) models and ADMS Verilog-A models have a very similar structure, implying that EDD models can be used as prototypes prior to compilation and linking via the compact device modelling route using ADMS. Once again a special thanks to Stefan Jahn for all his help and encouragement over the period that I have been developing the Verilog-A version of the operational amplifier macromodel, writing this report and testing the examples it includes.
3 Verilog-A Logarithmic Amplifier Macromodel

3.1 Introduction

The development of simulation component and device models in many ways reflects how circuit simulator functionality has improved with increasing personal computer computational power. Early circuit simulators were often restricted to the DC, AC and transient analysis domains. Similarly, in the early days of circuit simulation, the available types of component and device models were extremely limited, often being confined to the fundamental passive components, simple voltage and current sources and the basic semiconductor devices. Adding new models to a circuit simulator was, in most instances, a complex task. Today this picture is changing. Modern circuit simulators, like Qucs, are equipped with an ever widening selection of simulation tools plus increasingly sophisticated modelling tools. The later allows easy construction of subcircuit models, linear and non-linear macromodels, equation defined device models, and Verilog-A compact device models. This report describes how a compact macromodel of a logarithmic amplifier can be constructed from a model description written in the Verilog-A hardware description language, compiled to C++ code using the ADMS compiler plus Qucs XML interface, and linked to the main body of Qucs C++ code\(^1\). The logarithmic amplifier model demonstrates an approach to Qucs modelling which allows high-level functional models of integrated circuits to be added to the existing range of Qucs component and device models.

\(^1\)A detailed description of the procedure for the compilation of Verilog-A models with ADMS and linking of the resulting C++ code to Qucs can be found in the Qucs publication: “Qucs Description: Verilog-AMS interface”, by Stefan Jahn, Hélène Parisotte, located at http://qucs.sourceforge.net/docs.html.
3.2 The ideal logarithmic amplifier

The operation of an ideal logarithmic amplifier\(^2\) is defined by the function given in equation (3.1).

\[
V_{\text{out\(\text{(ideal)}\)}} = K_v \cdot \log \left( \frac{I_i}{I_r} \right)
\]  

(3.1)

The device accepts two input currents \(I_i\) and \(I_r\) and outputs voltage \(V_{\text{out\(\text{(ideal)}\)}}\) which is proportional to the base ten logarithm of the current ratio \(I_i/I_r\), where the constant of proportionality is \(K_v\) volts per decade. In equation (1) current \(I_r\) is called the reference current and current \(I_i\) represents the amplifier input signal. The primary purpose of a logarithmic amplifier is not to amplify input signals but to compress a wide dynamic range input signal to give as output it’s logarithmic equivalent. In some respects the name logarithmic amplifier is misleading and it would be better to consider the amplifier as a measurement device rather than an amplifier. For the ideal logarithmic amplifier when \(I_i = I_r\), the output voltage \(V_{\text{out\(\text{(ideal)}\)}} \Rightarrow 0\). In a practical logarithmic amplifier the current input terminals are effectively at virtual ground potential which allows the amplifier input signals to be derived from input voltages divided by scaling resistors of identical value. In this case \(I_r = V_r/R\) and \(I_i = V_i/R\), where \(V_r\) and \(V_i\) are the input signal voltages respectively, and \(R\) is the scaling resistance. Transforming from current inputs to voltage inputs gives equation (3.2).

\[
V_{\text{out\(\text{(ideal)}\)}} = K_v \cdot \log \left( \frac{V_i}{V_r} \right)
\]

(3.2)

To prevent the argument of the logarithmic amplifier from becoming negative the input signal \(I_i\) must always have the same polarity as reference signal \(I_r\). The amplitude of the signal at terminal \(I\) must also be the same or greater than the signal at terminal \(R\). This implies that logarithmic amplifiers are unipolar input devices. Similarly, to prevent the logarithmic amplifier output voltage from becoming excessively large and causing the output voltage to saturate\(^3\) the ratio of the two currents must be limited to a maximum value. In this context the dynamic range of a logarithmic amplifier is defined by equation (3.3).

\[
\text{dynamic range} \simeq \log \left( \frac{I_i}{I_r} \right) \simeq \log \left( \frac{V_i}{V_r} \right)
\]

(3.3)


\(^3\)Power supply voltages are often limited to \(\pm 15\) volts.
In a real logarithmic amplifier, \( I_r \) can be as low as 10 nA with the maximum allowed value of \( I_i \) around 10 mA, yielding a dynamic range of six decades. Integrated logarithmic amplifiers are available with dynamic ranges of five or six decades.

### 3.3 The practical logarithmic amplifier

The voltage output from a practical logarithmic amplifier\(^4\) differs from that given in equation (3.1) and can be written as

\[
V_{\text{out}} = V_{\text{out}(\text{ideal})} \pm TE
\]  
\[(3.4)\]

Where \( TE \) is called the total error. This can be represented by a function formed from the combination of errors in gain scale factor, input offset current, input bias current, output offset voltage and transfer function non-linearity. On adding the major contributions due to these errors, equation (3.4) becomes equation (3.5).

\[
V_{\text{out}} = K_v \cdot (1 \pm \Delta K_v) \cdot \log \left( \frac{I_i - I_{b1}}{I_r - I_{br}} \right) \pm 2 \cdot K_v \cdot N \cdot m \pm V_{\text{osout}}
\]  
\[(3.5)\]

In terms of voltage inputs, equation (3.5) can be written as

\[
V_{\text{out}} = K_v \cdot (1 \pm \Delta K_v) \cdot \log \left( \frac{V_i - I_{b1}}{R} \right) \pm 2 \cdot K_v \cdot N \cdot m \pm V_{\text{osout}}
\]  
\[(3.6)\]

Where \( \Delta K_v \) is the scale error factor in percent, \( I_{b1} \) is the bias current at input \( I \) in amperes, \( I_{br} \) is the bias current at the reference input \( R \) in amperes, \( N \) is the log conformity error in percent, \( m \) is the number of decades over which \( N \) is specified, and \( V_{\text{osout}} \) is the output offset voltage. The log conformity error of a logarithmic amplifier is defined as the peak deviation from the best-fit straight line of \( V_{\text{out}} \) versus the \( \log(I_i/I_r) \) curve expressed as a percentage of peak-to-peak full-scale. The other error parameters have their usual meaning. In general, error parameters may be plus or minus in sign, leading to the \( \pm \) signs in the previous equations.

### 3.4 Logarithmic amplifier temperature effects

The error parameters introduced in the last section of this report are normally specified in manufacturers device data sheets as functions of temperature. As a

---

\(^4\) See the manufacturers data sheets for (a) Burr Brown (from Texas Instruments) LOG100 and LOG101 amplifiers, and (b) Maxim MAX4206 amplifier.
first approximation parameter temperature dependence is usually limited to the simple linear functions of temperature given in equation (3.7).

\[
\Delta K_v (\text{Temp}) = \Delta K_v \cdot + \Delta K_v \text{tc} \cdot (\text{Temp} - T_{\text{nom}})
\]

\[
I_{b1} (\text{Temp}) = I_{b1} + I_{b1 \text{tc}} \cdot (\text{Temp} - T_{\text{nom}})
\]

\[
I_{br} (\text{Temp}) = I_{br} + I_{br \text{tc}} \cdot (\text{Temp} - T_{\text{nom}})
\]

\[
N (\text{Temp}) = N + N \text{tc} \cdot (\text{Temp} - T_{\text{nom}})
\]

\[
V_{\text{osout}} (\text{Temp}) = V_{\text{osout}} + V_{\text{osout} \text{tc}} \cdot (\text{Temp} - T_{\text{nom}})
\]

(3.7)

Where \(\text{Temp}\) is the circuit simulation temperature in Celsius, \(T_{\text{nom}}\) is the device parameter measurement temperature in Celsius and \(\Delta K_v \text{tc}, I_{b1 \text{tc}}, I_{br \text{tc}}, N \text{tc}\) and \(V_{\text{osout} \text{tc}}\) are first order linear temperature coefficients in percentage per degree Celsius or units per degree Celsius.

### 3.5 A compact macromodel for a logarithmic amplifier

#### 3.5.1 Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
<th>Default*</th>
</tr>
</thead>
<tbody>
<tr>
<td>(K_v)</td>
<td>(K_v)</td>
<td>Gain scale factor</td>
<td>V/decade</td>
<td>1.0</td>
</tr>
<tr>
<td>(D_k)</td>
<td>(\Delta K_v)</td>
<td>Gain scale factor error</td>
<td>%</td>
<td>0.3+</td>
</tr>
<tr>
<td>(I_{b1})</td>
<td>(I_{b1})</td>
<td>Bias current at input I</td>
<td>A</td>
<td>5e-12</td>
</tr>
<tr>
<td>(I_{br})</td>
<td>(I_{br})</td>
<td>Bias current at reference input R</td>
<td>A</td>
<td>5e-12</td>
</tr>
<tr>
<td>(M)</td>
<td>(M)</td>
<td>Number of decades over which N is specified</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>(N)</td>
<td>(N)</td>
<td>Log conformity error</td>
<td>%</td>
<td>0.1+</td>
</tr>
<tr>
<td>(V_{\text{osout}})</td>
<td>(V_{\text{osout}})</td>
<td>Output offset voltage</td>
<td>V</td>
<td>3e-3+</td>
</tr>
<tr>
<td>(R_{\text{inp}})</td>
<td>(R_{\text{inp}})</td>
<td>Amplifier input resistance</td>
<td>Ω</td>
<td>1e6</td>
</tr>
<tr>
<td>(F_c)</td>
<td>(F_c)</td>
<td>Amplifier voltage gain 2dB frequency</td>
<td>Hz</td>
<td>1e3</td>
</tr>
<tr>
<td>(R_o)</td>
<td>(R_o)</td>
<td>Amplifier output resistance</td>
<td>Ω</td>
<td>1e-3</td>
</tr>
<tr>
<td>(N \text{tc})</td>
<td>(N \text{tc})</td>
<td>Log conformity error temperature coefficient</td>
<td>%/Celsius</td>
<td>0.002</td>
</tr>
<tr>
<td>(V_{\text{osout} \text{tc}})</td>
<td>(V_{\text{osout} \text{tc}})</td>
<td>Output offset voltage temperature coefficient</td>
<td>V/Celsius</td>
<td>80e-6</td>
</tr>
<tr>
<td>(Dk \text{tc})</td>
<td>(\Delta K_v \text{tc})</td>
<td>Gain scale factor temperature coefficient</td>
<td>%/Celsius</td>
<td>0.03</td>
</tr>
<tr>
<td>(I_{b1 \text{tc}})</td>
<td>(I_{b1 \text{tc}})</td>
<td>Input I bias current temperature coefficient</td>
<td>A/Celsius</td>
<td>0.5e-12+</td>
</tr>
<tr>
<td>(I_{r \text{tc}})</td>
<td>(I_{r \text{tc}})</td>
<td>Input R bias current temperature coefficient</td>
<td>A/Celsius</td>
<td>0.5e-12+</td>
</tr>
<tr>
<td>(T_{\text{nom}})</td>
<td>(T_{\text{nom}})</td>
<td>Parameter measurement temperature</td>
<td>Celsius</td>
<td>26.85</td>
</tr>
</tbody>
</table>

* The default parameters are for a typical integrated circuit logarithmic amplifier.
+ These parameters may be negative.
++ Typical bias current doubles for every eight to ten degrees temperature increase.

### 3.5.2 Verilog-A model code

```verilog
// Qucs generic logarithmic amplifier model:
// This model can be used to construct working models for
// a range of different manufacturer's logarithmic amplifier ICs —
// for example the LOG100 and the MAX4206.
// All required parameters can be extracted directly from manufacturers data sheets.
// The structure and theoretical background to the logarithmic amplifier
// Verilog—a model are presented in the Qucs log_amp report.
//
// This is free software; you can redistribute it and/or modify
// it under the terms of the GNU General Public License as published by
// the Free Software Foundation; either version 2, or (at your option)
// any later version.
//
// Copyright (C), Mike Brinson, mbrin72043@yahoo.co.uk, January 2008.

'include "disciplines.vams"
'include "constants.vams"
module log_amp (P_I1, P_Ir, P_Vout);
  inout P_I1, P_Ir;
  inout P_Vout;
  //
  // Internal nodes
  //
  electrical n3, n4;
  //
  'define attr (txt) (*txt*)
  //
  parameter real Kv = 1.0 from [-inf : inf]
    'attr (info="scale_factor" unit = "V/decade")
    'attr (info="scale_factor_error" unit = "%")
  ;
  parameter real Dk = 0.3 from [-100 : 100]
    'attr (info="input_I1_bia  s_current" unit = "A")
  ;
  parameter real Ib1 = 5e-12 from [-inf : inf]
    'attr (info="input_I1_bia  s_current" unit = "A")
  ;
  parameter real Ib2 = 5e-12 from [-inf : inf]
    'attr (info="input_Ir_  eference bias_current" unit = "A")
  ;
  parameter real M = 5 from [1 : inf]
    'attr (info="number_of_decades")
  ;
  parameter real N = 0.1 from [0 : 100]
    'attr (info="conformity_error" unit = "%")
  ;
  parameter real Vosout = 3e-3 from [-inf : inf]
    'attr (info="output_offset_error" unit = "V")
  ;
  parameter real Rinp = 1e6 from [1 : inf]
    'attr (info="amplifier_input resistance" unit = "Ohm")
  ;
  parameter real Fe = 1e3 from [1 : inf]
    'attr (info="amplifier_3dB_frequency" unit = "Hz")
  ;
  parameter real Ro = 1e-3 from [1e-3 : inf]
    'attr (info="amplifier_output_resistance" unit = "Ohm")
  ;
  parameter real Ntc = 0.002 from [-100 : 100]
    'attr (info="conformity_error_temperature_coefficient" unit = "/Celsius")
  ;
  parameter real Vosouttc = 80e-6 from [-inf : inf]
    'attr (info="offset_temperature_coefficient" unit = "V/Celsius")
  ;
```

63
parameter real Dktc = 0.03 from [-100 : 100]
  'attr(info="scale_factor_error_temperature_coefficient" unit ="%/Celsius");
parameter real Ib1tc = 0.5e-12 from [-inf : inf]
  'attr(info="input_bias_current_temperature_coefficient" unit ="A/Celsius");
parameter real Ibrtc = 0.5e-12 from [-inf : inf]
  'attr(info="input_reference_bias_current_temperature_coefficient" unit ="A/Celsius");
parameter real Tnom = 26.85 from [-273 : inf]
  'attr(info="parameter_measurement_temperature" unit ="Celsius");
//
real R, Ix;
real V1, V2;
real Cc, PI;
real TempK, TnomK, Tdiff, NTemp, VosoutTemp, DkTemp, Ib1Temp, IbrTemp;
// analog begin
// // Constants
// PI=3.14159265358979323846;
// // Model equations
// // V1=V(P_I1);
// V2=V(P_Ir)+1e-20;
// R=Rinp+1e-6;
// Cc=1/(2*PI*Fc);
// TempK=$temperature;
// TnomK=Tnom+273.15;
// Tdiff=TempK-TnomK;
// NTemp=N+Ntc*Tdiff;
// VosoutTemp=Vosout+Vosouttc*Tdiff;
// DkTemp=Dk+Dktc*Tdiff;
// Ib1Temp= Ib1+Ib1tc*Tdiff;
// IbrTemp= Ibr+Ibrtc*Tdiff;
// if (V1 >= V2 ) Ix = Kv*(1+DkTemp/100)*log (((V1/R)-Ib1Temp)/(V2/R)-IbrTemp))+
// (Kv*2*(NTemp/100)*M)+VosoutTemp ;
else Ix = 0.0;
// // Circuit stages
// // Input stage
// I(P_I1) <+ V(P_I1)/R;
// I(P_Ir) <+ V(P_Ir)/R;
// // Log function stage
// I(n3) <+ -Ix;
// I(n3) <+ V(n3);
// // Frequency compensation
// I(n4) <+ -V(n3);
// I(n4) <+ V(n4);
// I(n4) <+ ddt(Cc*V(n4));
// // Output stage
// I(P_Vout) <+ -V(n4)/Ro;
// I(P_Vout) <+ V(P_Vout)/Ro;
//
3.6 Basic logarithmic amplifier operation

The circuit shown in Fig. 3.1 demonstrates the operation of the logarithmic amplifier macromodel with the input signals set as voltages. Input scaling resistance $R_{inp}$ is 10kΩ, the reference voltage is 100 uV DC (which is equivalent to $I_r = 10$ nA), and the input signal $V_s$ is swept between 1 uV and 10 V DC. For input signals ($V_2$) less than $V_1$ the macromodel restricts the output voltage to zero volts, preventing signal ratios from being less than one. Figure 3.2 illustrates the logarithmic amplifier operating in current input mode. In Fig. 3.2 the input scaling resistors are set to 1Ω, causing the amplifier inputs to become effectively virtual earth points. Both Fig. 3.1 and Fig. 3.2 illustrate the performance of a typical general purpose logarithmic amplifier over five signal decades, clearly showing the signal compression properties of the device.
Figure 3.1: Qucs schematic for a basic voltage driven logarithmic amplifier and simulated DC transfer function

Figure 3.2: Qucs schematic for a basic current driven logarithmic amplifier and simulated DC transfer function
### 3.7 Functional description of the Verilog-A logarithmic amplifier macromodel

The macromodel of a general purpose logarithmic amplifier presented in previous sections simulates the following device characteristics:

- **Input stage**: Scaling resistances and DC bias currents.
- **Gain stage**: Logarithmic base ten transfer function over \( N \) decades with a single pole frequency response. Errors; gain scale and log conformity.
- **Output stage**: Resistance and DC offset voltage.
- **Properties with temperature variation**: gain scale, log conformity, bias currents and output offset voltage.

#### 3.7.1 Input stage

The input stage is represented by the Verilog-A code listed in this subsection of the report. The voltages at input terminals \( P_{I_1} \) and \( P_{I_r} \) are divided by scaling resistors \( R \) to give the required input currents. When \( R \) is small the input stage operates in current mode.

```verilog-a
// Input stage
I(P_{I1}) <- V(P_{I1})/R;
I(P_{Ir}) <- V(P_{Ir})/R;
```

#### 3.7.2 Gain stage

The gain stage is represented by the Verilog-A code listed in this subsection of the report. This part of the model determines the primary logarithmic amplifier transfer function, including logarithmic characteristics, frequency response, errors and temperature effects. An if-else statement is used to test if the log function argument is greater than one, setting the transfer function output to zero when the test fails. Both error terms and temperature factors have been included in the amplifier transfer function equation. Logarithmic amplifier transfer function frequency response is normally a complex function of input currents and an internal frequency compensation capacitance. Manufacturer’s data sheets usually provide curves of frequency response for typical values of input current and compensation capacitance. Frequency effects are represented in the macromodel by a single pole response. The 3dB corner frequency being set by device parameter \( Fc \). The default value of 3 kHz should be changed to suit the circuit operating conditions.
Figure 3.3 illustrates a small signal test circuit which allows amplifier transfer function frequency response to be simulated.

```verbatim
//
// Constants
//
PI=3.14159265358979323846;

// Model equations
//
V1=V(P_I1);
V2=V(P_Ir)+1e-20;
R=Rp+1e-6;
Cc=1/(2*PI*Fc);

//
TempK=$temperature;
TnomK=Tnom+273.15;
Tdiff=TempK-TnomK;
NTemp=N+Ntc*Tdiff;
VosoutTemp=Vosout+Vosouttc*Tdiff;
DkTemp=Dk+Dktc*Tdiff;
Ib1Temp=Ib1+Ib1tc*Tdiff;
IbrTemp=Ibr+Ibrtc*Tdiff;

// if (V1>=V2 ) Ix = Kv*(1+DkTemp/100)*log (((V1/R)-Ib1Temp)/((V2/R)-IbrTemp))+(Kv*2*(NTemp/100)*M)+VosoutTemp ;
else Ix = 0.0;
.
.
.
// Log function stage
//
I(n3)<-Ix;
I(n3)<-V(n3);

// Frequency compensation
//
I(n4)<-V(n3);
I(n4)<-V(n4);
I(n4)<-ddt(Cc*V(n4));
```

### 3.7.3 Output stage

The output stage is represented by the Verilog-A code listed in this subsection of the report. This final section of the model introduces an output resistance $R_0$. In a practical logarithmic amplifier this is often low in value.

```verbatim
// Output stage
I(P_Vout)<-V(n4)/Ro;
I(P_Vout)<-V(P_Vout)/Ro;
```
3.8 Logarithmic amplifier large signal AC response

The circuit and waveforms presented in Fig. 3.4 illustrate how the large signal AC response of a logarithmic amplifier can be tested and displayed. In this circuit a 100 Hz, 1.9 V peak sinewave signal, in series with a 2V battery, is applied to amplifier input I. Amplifier reference R has a 0.1V battery connected as the reference signal. As the logarithmic amplifier output signal is proportional to the log of the ratio of the input signals $I/R$, the shape of resulting output signal differs considerably from that of the excitation sinewave. When the peak of the input sinewave is 1.9 V the input ratio is 29 and when the negative peak reaches -1.9 V, the ratio is 1, yielding an output waveform with signal values between log(29) and 0. This example test circuit once again demonstrates the compression properties of logarithmic amplifiers.
3.9 Logarithmic amplifier transfer function

temperature variation

The test circuit shown in Fig. 3.5 introduces a double sweep which changes the amplifier circuit temperature from -110 to 100 Celsius, while simultaneously at each temperature, simulates, records and displays the amplifier transfer function. In this very basic example of amplifier response to temperature changes all circuit dependent parameters are varied at the same time and no attempt is made to identify individual parameter contributions to the overall temperature dependency. From the results of this simple test the simulation waveforms indicate that the typical temperature coefficients only have minimal effect on circuit performance. Modern integrated logarithmic amplifiers are, in general, well temperature compensated, minimising the effects of temperature changes on circuit performance.
3.10 Logarithmic amplifier applications

In this section of this brief report two applications of the logarithmic amplifier are introduced. These examples are also used to demonstrate how Verilog-A modelled devices can be merged with other Qucs built-in components, subcircuits and equation defined devices. The application examples have been chosen to illustrate the power of Qucs modelling and simulation.

3.10.1 A simple signal multiplier

One of the most basic, and earliest, applications of the logarithmic amplifier was signal multiplication. Figure 3.6 shows a test circuit which includes two logarithmic amplifiers, two voltage controlled voltage sources (these act as a voltage summer) and an antilog amplifier.

The circuit illustrated in Fig. 3.6 multiplies the ratios of the two sets of inputs. This is done by taking the log of each input ratio then adding the results and finally finding the antilog of the sum. The antilog of a voltage can be found using the circuit shown in Fig. 3.7. Parameters Ir and K are used to scale the output voltage. This must be within the power supply range of a practical device. In the example shown in Fig. 3.6 the second input ratio is constant at 4 and the first has
a maximum value of $10/1e^{-3} = 1e4$, causing the output result to be $4e4$ which is way beyond the output voltage of a practical circuit. By setting $k=1$ and $I_r$ to $1e-4$ the output voltage is scaled so that the maximum output becomes roughly 4 volts.

### 3.10.2 Light absorption measurements using photodiodes and a log amplifier

A number of years ago a colleague in Germany made the profound remark that the 20th century was the century of the electron and that the 21st century was likely to be the century of the photon. The current state of Qucs model development does to some extent reflect this thinking. At present the major modelling tasks involve extending the Qucs component/model range and the improvement of their indi-
Figure 3.7: A simple antilog amplifier based on a single equation defined device:
Controlled source SRC2 acts as a buffer and source SCR1 converts EDD current I1 to voltage

vidual performances. Looking through the current device/model list immediately confirms that it is dominated by electrical components and other domain devices, such as transducers, actuators and optical components, are non-existant. The logarithmic amplifier application reported here attempts to address this imbalance by providing some preliminary information on an area of modelling where significant work is likely to be done in the coming cycles of Qucs development, namely optical components. Optoelectronic devices, such as LEDs and photodiodes, are well established in the current electronics scene. Unfortunately, to my knowledge, Qucs lacks the models for such devices. The test circuit shown in Fig. 3.8 presents a basic arrangement for measuring the light absorption properties of liquids. This is a classical application of the logarithmic amplifier, working as a device that measures the ratio of two currents. These currents are generated by photodiodes.

In Fig. 3.8 a light source shines on two photodiodes: directly on one and indirectly on the other. In the second case the light travels through a vessel containing a liquid which attenuates the light. The level of attenuation being dependent on the light absorption properties of the liquid. When little or no light is absorbed the logarithmic amplifier output is small. However, at high light absorption levels the amplifier output is high. The circuit given in Fig. 3.8 works over six decades of light transmission coefficient. Moreover, it does not require the absolute values of the light intensities to be measured. The circuit output voltage is compressed to a range between 0 and 5 volts which is ideal for interfacing with a unipolar analogue-to-digital converter. Qucs cannot represent light signals directly. However, it is possible to use a voltage to represent the intensity of a light. Once one realises that the numerical value of light intensity can be represented by a voltage of the
same numerical value then it also becomes possible to represent light signals paths by nets with specific voltage values. In Fig. 3.8 the light paths are represented by wires connecting the light source, the liquid vessel and the photodiodes. Models for the light absorbing liquid and the photodiodes are shown in Fig. 3.9.

![Diagram](image)

Figure 3.8: Light absorption measurements using photodiodes and a logarithmic amplifier

In Fig. 3.9 the light absorbing liquid is represented by a voltage controlled voltage source where the source gain models the transmission coefficient: a gain of one implies 100% transmission and a gain of zero no light transmission at all. The photodiode model is much more complex. A voltage controlled current source in parallel with a diode forms the core of the model. The gain of the controlled source represents the responsivity of the diode. Responsivity is expressed in amperes per watt or as the photodiode current for a given input light power per unit area. As the current generated is also expressed as the current per unit area, effectively...
the area factor is eliminated. Equation (3.8) relates the photodiode current to the voltage at the light input terminal:

\[ I_d = \text{Responsivity} \cdot V(PV_{\text{light}}) \]  

(3.8)

Responsivity is a function of the light wavelength and is around 0.5 to 0.6 for wavelengths of 900nm. It is roughly 0.3 for blue wavelengths and drops to 0.2 in the ultraviolet region of the spectrum. With no illumination falling on a photodiode the resulting diode current is small, being called the device dark current. It ranges from tens of pA for ultraviolet detecting photodiodes to several \(\mu\text{A}\) for low cost silicon diodes. Typical values for \(R_{\text{series}}\) are in the range 1m to 20m\(\Omega\). The other parameters are similar to those representing standard semiconductor diodes but with values specifically chosen to represent the properties of photodiodes.

3.11 End note

These notes summarise a basic technique for modelling logarithmic amplifiers using Verilog-A. Verilog-A is primarily intended for modelling compact semiconductor devices. However, as this report demonstrates it can be equally employed for macromodelling of integrated circuits and circuits in general. The Qucs C++ code for the modular operational amplifier model, generated by ADMS, can be

Figure 3.9: Experimental Qucs models for a light absorbing liquid and a photodiode
found in the Qucs release archives at http://qucs.sourceforge.net/download.html. The procedure undertaken to convert the Verilog-A code into C++ for compilation and linking with Qucs closely followed that described by Stefan Jahn and Hélène Parruitte. Although it takes more work to construct models using ADMS the effort is worthwhile because the finished models are very efficient in terms of memory usage and have significantly reduced run times. It is worth noting that Verilog-A based models can be combined with other forms of Qucs model, forming a powerful combination that extends Qucs simulation capabilities. Once again a special thanks to Stefan Jahn for all his help and encouragement over the period that I have been developing the Verilog-A logarithmic amplifier macromodel, writing this report and testing the examples it includes.
4 Verilog-A Macromodel for Resistive Potentiometers

4.1 Introduction

The resistive potentiometer is a common component in electronic systems. Unfortunately, it is often very poorly modelled by circuit simulators. A common approach is to simply treat the device as two series resistances with values set by linear or logarithmic algebraic equations. This is fine as a rough and ready approach to modelling the basic potentiometer function. However, it fails to acknowledge the fact that potentiometers are much more complex devices that involve not only electrical characteristics but also mechanical rotational features. Furthermore, potentiometers are subject to a number of errors such as taper conformity and linearity. This report presents a more realistic model of a resistive potentiometer and shows how Qucs can be used to develop practical models of this fundamental component that give an order of magnitude improvement over the commonly used two resistor models. Finally, the notes show how a Qucs subcircuit of the potentiometer can be coded as a compact Verilog-A macromodel.

4.2 The two resistor potentiometer model

The schematic for a two resistor model of a linear resistive potentiometer is shown in Fig. 4.1. Sweep parameter Position is used to control the movement of the potentiometer central output terminal. A range of zero to one covers the movement of the output terminal from one end of the potentiometer to the other. This model acts more like a sliding arm potentiometer rather than the more common rotary type. Notice the use of non-integer values 1.00001 and 0.00001 to ensure that R1 or R2 do not become zero in value when the mid-terminal is slid to either end of the potentiometer. Changing equations R1eqn and R2eqn allows different laws to be specified that relate the values of resistors R1 and R2 to the position of the mid-terminal.
Figure 4.1: Basic two resistor model of a linear resistive potentiometer

4.3 Potentiometer types

The basic types of resistive potentiometer are the rotary and slider forms\(^1\). These are constructed from wire, cemet or conductive plastic resistive strips attached to a suitable non-conducting holder with fixed contacts at the ends and a moveable wiper contact. The moveable contact either traverses in a rotary direction or in a straight line. The resistive strip has either a constant width or is shaped depending on the type of potentiometer, giving either constant resistance or changing resistance per unit length along the length of a potentiometer. Probably the most common of the non-linear types of potentiometer is the logarithmic potentiometer. Figure 4.2 illustrates how linear, logarithmic and inverse logarithmic device laws vary as a function of wiper contact angle. Logarithmic potentiometers are sometimes called audio potentiometers due to their use as volume control devices in audio amplifiers. Potentiometers with logarithmic resistive laws are necessary because the human ear responds to the logarithm of loudness, making control of amplifier output level smoother with a logarithmic potentiometer rather than the simpler linear device. The shape of the potentiometer response law is often called the potentiometer taper. Today linear potentiometers are the most common type made by different manufacturers. One reason for this is the cost of manufacturing a true logarithmic law device. In many cases so called logarithmic potentiometers are in fact simpler devices constructed from two different sections of resistive material where the low angle part of the potentiometer track has a smaller resistivity than the high angle section. Logarithmic potentiometers are normally specified as

20% or 10% types, being defined as the percentage of total potentiometer resistance between the bottom fixed contact and the wiper contact when the wiper is moved to the middle of its full range. Inverse logarithmic potentiometers have a similar characteristic to the logarithmic potentiometer except that potentiometer taper is reversed. This has the effect of causing large changes in output at small wiper angles and the reverse at high angles. Inverse logarithmic potentiometers have in recent years become unusual items and are no longer widely manufactured.

![Figure 4.2: Resistive potentiometer characteristics: Vin = 1V DC](image)

### 4.4 Modelling potentiometer taper laws

Due to their lower cost, and availability, linear potentiometers are often chosen as a starting point when designing a circuit that requires a potentiometer with a specific taper law. The same applies to modelling potentiometers with a known resistive taper. By adding a fixed resistance, external to a potentiometer, a linear potentiometer can be converted to one with a designer specified taper. Consider the three resistor diagram shown in Fig. 4.3.

The transfer function for the schematic illustrated in Fig. 4.3 is given in equation (4.1).

\[
\frac{V_{out}}{V_{in}} = \frac{(R_2 \parallel R_T)}{R_1 + (R_2 \parallel R_T)} = \frac{1}{1 + \frac{R_1}{R_T} + \frac{R_1}{R_T}}
\]  

(4.1)

Writing \( R_{pot} = R_1 + R_2 \) and setting \( a = R_2/R_{pot} \) and \( TaperCoeff = R_T/R_{pot} \) yields equation (4.2).
Figure 4.3: Basic two resistor potentiometer with taper resistor RT connect between the bottom fixed contact (B) and the wiper arm contact (M)

\[
\frac{V_{out}}{V_{in}} = \frac{1}{1 + \frac{1-a}{a} + \frac{1-a}{TaperCoeff}} = \frac{a \cdot TaperCoeff}{a - a^2 + TaperCoeff} \tag{4.2}
\]

Where \(TaperCoeff\) is the potentiometer taper coefficient (a fixed value greater than zero) and parameter \(a\) is a measure of the wiper arm position (being in the range 0 to 1). As the taper coefficient approaches a large value (much greater than one) the potentiometer law approaches that of a simple linear potentiometer, effectively this implies that \(R_T >> R_{pot}\). For rotary potentiometers, parameter \(a\) can also be expressed as \(a = \frac{\text{Angle}}{\text{MaxAngle}}\). In the case of a single turn potentiometer \(0 <= \text{Angle} <= 360\) degrees and \(\text{MaxAngle} = 360\) degrees. Figure 4.4 illustrates the effect of different \(TaperCoeff\) values on the potentiometer response curves. Logarithmic potentiometer response is approximated when the \(TaperCoeff\) is in the range 0.2 to 0.25.
4.5 Modelling inverse logarithmic potentiometers

By placing the fixed taper resistance in parallel with resistor R1 the potentiometer response changes to the inverse logarithmic form shown in Fig. 4.2. Consider the three resistor model shown in Fig. 4.5.

![Figure 4.5: Basic two resistor potentiometer with taper resistor RT connect between the top fixed contact (T) and the wiper arm contact (M)](image)

The transfer function for the schematic illustrated in Fig. 4.5 is given in equation (4.3).
\[ \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_2}{(R_1 \parallel R_T) + R_2} = \frac{R_2}{\left(\frac{R_1 \cdot R_T}{R_1 + R_T}\right) + R_2} = \frac{R_1 \cdot R_2 + R_2 \cdot R_T}{R_1 \cdot R_2 + R_1 \cdot R_T + R_2 \cdot R_T} \]  

(4.3)

Writing \( R_{\text{pot}} = R_1 + R_2 \) and setting \( a = \frac{R_2}{R_{\text{pot}}} \) and \( \text{TaperCoeff} = \frac{R_T}{R_{\text{pot}}} \) yields equation (4.4).

\[ \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{a - a^2 + a \cdot \text{TaperCoeff}}{a - a^2 + \text{TaperCoeff}} \]  

(4.4)

Figure 4.6 illustrates the effect of different \( \text{TaperCoeff} \) values on the inverse potentiometer response curves. Inverse logarithmic potentiometer response is approximated when the \( \text{TaperCoeff} \) is in the range 0.2 to 0.25.

Figure 4.6: Inverse potentiometer response curves for different \( \text{TaperCoeff} \) values: curves blue to black; \( \text{TaperCoeff} = 0.1, 0.2, 0.75, 1, 2, 3, 4, 5 \)

4.6 A Qucs subcircuit model of a resistive potentiometer

The schematic for a resistive potentiometer modelled as a Qucs subcircuit is shown in Fig. 4.7. This model is based on the background ideas and theory presented in
the previous sections of this report. The subcircuit schematic represents a practical resistive potentiometer, with electrical and positional characteristics set by a resistive taper coefficient, a conformity error parameter, a linearity parameter, wiper arm contact resistance and resistance temperature coefficient. The subcircuit models both single and multi-turn potentiometers of type linear, logarithmic or inverse logarithmic and indeed any other laws set by the value of parameter Taper_Coeff. The following list outlines the function and units of the model parameters.

### 4.6.1 Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
<th>Default*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rpot</td>
<td>$R_{pot}$</td>
<td>Nominal device resistance</td>
<td>Ω</td>
<td>1e4</td>
</tr>
<tr>
<td>Rotation</td>
<td>$Rotation$</td>
<td>Shaft/wiper arm rotation</td>
<td>degrees</td>
<td>120</td>
</tr>
<tr>
<td>Taper_Coeff</td>
<td>$TaperCoeff$</td>
<td>Resistive law taper coefficient</td>
<td>%</td>
<td>0</td>
</tr>
<tr>
<td>LEVEL</td>
<td>$LEVEL$</td>
<td>Device type selector</td>
<td>%</td>
<td>1+</td>
</tr>
<tr>
<td>Temp</td>
<td>$Temp$</td>
<td>Circuit temperature</td>
<td>Celsius</td>
<td>26.85</td>
</tr>
<tr>
<td>Max_Rotation</td>
<td>$MaxRotation$</td>
<td>Maximum shaft/wiper rotation</td>
<td>degrees</td>
<td>240+</td>
</tr>
<tr>
<td>Conformity</td>
<td>$Conformity$</td>
<td>Conformity error</td>
<td></td>
<td>0.2</td>
</tr>
<tr>
<td>Linearity</td>
<td>$Linearity$</td>
<td>Linearity error</td>
<td>%</td>
<td>0.2</td>
</tr>
<tr>
<td>Tnom</td>
<td>$T_{nom}$</td>
<td>Parameter measurement temperature</td>
<td>Celsius</td>
<td>26.85</td>
</tr>
<tr>
<td>Contact_Res</td>
<td>$ContactRes$</td>
<td>Wiper arm contact resistance</td>
<td>Ω</td>
<td>1</td>
</tr>
<tr>
<td>Temp_Coeff</td>
<td>$TempCoeff$</td>
<td>Resistance temperature coefficient</td>
<td>PPM/Celsius</td>
<td>100+++</td>
</tr>
</tbody>
</table>

* The default parameters are for typical 10k cemet linear potentiometer.
+ Parameter LEVEL selects the potentiometer type: LEVEL=1; linear, LEVEL=2; logarithmic and LEVEL=3; inverse logarithmic.
++ For a single turn potentiometer 240 $\leq$ MaxRotation $\leq$ 360 degrees. For multi-turn potentiometers add 360 degrees per complete shaft rotation.
+++ Potentiometer temperature coefficients are normally quoted in parts per million (PPM) per degree Celsius by manufacturers. Typical values are: cemet $\pm$100 PPM/Celsius, wire $\pm$50 PPM/Celsius and conductive plastic $\pm$1000 PPM/Celsius.

Potentiometer functional errors are introduced in the model illustrated in Fig. 4.7 by adding conformity and linearity factors to the basic taper coefficient via equation (4.5).

---

2The value of parameter MaxRotation is normally set by the position of an end stop at the end of the resistive track.
\[ Tpcoeff = TaperCoeff + \frac{Conformity + Linearity \cdot \sin (RadAngle)}{100} \]  (4.5)

Where \( RadAngle = Rotation \cdot \pi/180 \) is the shaft rotation angle in radians. Absolute conformity error is defined as the maximum deviation of the taper function characteristic from an ideal theoretical characteristic. Conformity error is normally specified in percentage and can have plus or minus values. Absolute linearity has a similar definition. However, it often shows sinusoidal characteristics\(^3\) due to shaft rotation, particularly with multi-turn potentiometers. Contact resistance has been introduced into the model to take account of any resistance that exists from the wiper terminal to the contact on the potentiometer resistive track. With sprung loaded contacts this resistance should be small and can often be neglected. Effects of temperature on the model performance are included via a simple linear temperature coefficient which controls the change in device resistance as temperature varies. A potentiometer test circuit and the response of a multi-turn linear potentiometer with zero conformity and linearity errors are given in Fig. 4.8. Multi-turn potentiometers are modelled by setting the shaft rotation parameter to multiplies of 360 degrees plus slightly less angle for the final rotation. Figure 4.9 illustrates a test circuit for comparing the performance of log and inverse log single-turn potentiometers. The response curves show both simulation results and those obtained by fitting logarithmic curves to the simulated output data. With the Taper_Coeff parameter set to 0.2, remarkably good agreement is observed when the simulation data is compared to the ideal logarithmic performance. The test circuit and simulation curves illustrated in Fig. 4.10 demonstrate the effects that conformity and linearity parameters have on a multi-turn potentiometer. Normally both of these parameters are much less than one percent, making their effects difficult to observe. In Fig. 4.10 they have both been set at ten percent, greatly exaggerating their effect on potentiometer performance.

\(^3\)See section 3.2: Novotechnik Potentiometer Definitions, http://www.novotechnik.com/novotechnic_tech_ref.html
Figure 4.7: Qucs subcircuit of a resistive potentiometer: schematic, equations and symbol

Figure 4.8: Multi-turn linear potentiometer test circuit and performance curve
Figure 4.9: Single-turn log and inverse log potentiometer test circuit and performance curves: (1) simulated data solid curves, (2) fitted data dotted curves

Equation
Eqn 1
\[ V_{pot1} = 1 - \exp\left(\frac{\text{Max} - \text{Min} \cdot \text{Angle}}{\text{Min}}\right) \]
\( k = 0.66 \)
\( \text{Max} = 280 \)

Equation
Eqn 2
\[ V_{pot2} = k \cdot \log_{10}\left(\frac{\text{Angle} + \text{Min}}{\text{Min}}\right) \]
\( k = 0.66 \)
Figure 4.10: Multi-turn log potentiometer test circuit and response curves, illustrating conformity and linearity errors: both conformity and linearity parameters are set at ten percent to clearly indicate their effects; blue curve Pot1, red curve Pot2 and black curve Pot3.
4.7 A Verilog-A resistive potentiometer model

One of the advantages of using Qucs subcircuits, and indeed EDD models, is that they allow fast interactive prototyping of new models. Once a new model is tested and functioning satisfactorily it can often be easily translated into Verilog-A code for compiling into C++ code, using the ADMS compiler, and finally compiled and linked with the main Qucs software. When prototyping new models it is advisable to use, whenever possible, circuit elements/structures that can be easily transposed to Verilog-A statements. The Verilog-A code listed in the next section is based directly on the Qucs subcircuit model of the potentiometer. In general there is a one-to-one correspondence between the different sections of the subcircuit model and the Verilog-A code. However, for completeness the Verilog-A code also includes white noise statements to account for resistor noise. Overall the subcircuit model and the Verilog-A code give the same performance except that the Verilog-A code appears to simulate much faster. This is not surprising considering it comprises compiled and linked machine code rather than being a netlist which is interpreted during circuit simulation.

4.8 Verilog-A model code

```verilog
// Qucs resistive potentiometer model:
// This model can be used to construct working linear, logarithmic and inverse logarithmic
// potentiometers, or other devices with designer specified resistive taper functions.
// All required parameters can be extracted directly from
// manufacturers data sheets.
//
// The structure and theoretical background to the potentiometer
// Verilog-a model are presented in the Qucs potentiometer report.
//
// This is free software; you can redistribute it and/or modify
// it under the terms of the GNU General Public License as published by
// the Free Software Foundation; either version 2, or (at your option)
// any later version.
//
// Copyright (C), Mike Brinson, mbrin72043@yahoo.co.uk, February 2008.
//
#include "disciplines.vams"
#include "constants.vams"

module potentiometer (B, M, T);
    inout B, M, T;
    //
    // Internal nodes
    //
    electrical n1;
```

4 The resistors comprising the potentiometer subcircuit have thermal noise built-in as a standard component feature.
// 'define attr(txt) (*txt*)
//
// parameter real R_pot = 1e4 from [1e-6 : inf]
// 'attr(info="nominal_device_resistance" unit = "Ohm");
// parameter real Rotation = 120 from [0 : inf]
// 'attr(info="shaft/wiper_arm_rotation" unit = "degrees");
// parameter real Taper_Coeff = 0 from [0 : inf]
// 'attr(info="resistive_law_taper_coefficient" );
// parameter integer LEVEL = 1 from [1 : 3]
// 'attr(info="device_type_selector" );
// parameter real Max_Rotation = 240.0 from [0 : inf]
// 'attr(info="maximum_shaft/wiper_rotation" unit = "degrees");
// parameter real Conformity = 0.2 from [-inf : inf]
// 'attr(info="conformity_error" unit = "%");
// parameter real Linearity = 0.2 from [-inf : inf]
// 'attr(info="linearity_error" unit = "%");
// parameter real Contact_Res = 1 from [1e-6 : inf]
// 'attr(info="wiper_arm_contact_resistance" unit = "Ohm");
// parameter real Temp_Coeff = 100 from [0 : inf]
// 'attr(info="resistance_temperature_coefficient" unit = "PPM/Celsius");
// parameter real Tnom = 26.85 from [-273 : inf]
// 'attr(info="parameter_measurement_temperature" unit = "Celsius");
//
real Rad_Angle, R_pot_Temp, Rtop, Rbot, Tpcoeff, Rcontact;
real RTB, RTT, error_term;
real fourkt;
//
// analog begin
//
// Model equations
//
// Rcontact=Contact_Res+1e-6;
// Rad_Angle=Rotation*M_PI/180;
// R_pot_Temp=(R_pot+1e-6)/(1+Temp_Coeff*(temperature-Tnom)/1e6);
// Tpcoeff=Taper_Coeff+(Conformity+Linearity*sin(Rad_Angle))/100;
// error_term=(1+(Conformity+Linearity*sin(Rad_Angle))/100);
//
// case (LEVEL)
// 2: begin
//  RTB=R_pot_Temp*Tpcoeff;
//  RTT=1e15;
//  Rtop=(1.000001-(Rotation/(Max_Rotation+1e-20)))*R_pot_Temp;
//  Rbot=(0.000001+(Rotation/(Max_Rotation+1e-20)))*R_pot_Temp;
// end
// 3: begin
//  RTB=1e15;
//  Rtop=(1.000001-(Rotation/(Max_Rotation+1e-20)))*R_pot_Temp;
//  Rbot=(0.000001+(Rotation/(Max_Rotation+1e-20)))*R_pot_Temp;
// end
// default: begin
//  RTB=1e15;
//  RTT=1e15;
//  Rtop=(1.000001-(Rotation/(Max_Rotation+1e-20)))*R_pot_Temp*error_term;
//  Rbot=(0.000001+(Rotation/(Max_Rotation+1e-20)))*R_pot_Temp*error_term;
// end
//
// if (Taper_Coeff == 0.0)
RTB=1e15;
RTT=1e15;
Rtop=(1.000001−(Rotation/(Max_Rotation+1e−20)))*R_pot_Temp*error_term;
Rbot=(0.000001+(Rotation/(Max_Rotation+1e−20)))*R_pot_Temp*error_term;
end

// Macromodel
//
I(T, n1) <+ V(T, n1)/Rtop;
I(T, n1) <+ V(T, n1)/RTT;
I(B, n1) <+ V(B, n1)/Rbot;
I(B, n1) <+ V(B, n1)/RTB;
I(M, n1) <+ V(M, n1)/Rcontact;

// Noise contributions
//
fourkt=4.0*P_K*$temperature;
I(T, n1) <+ white_noise(fourkt/Rtop, “thermal”);
I(T, n1) <+ white_noise(fourkt/RTT, “thermal”);
I(B, n1) <+ white_noise(fourkt/Rbot, “thermal”);
I(B, n1) <+ white_noise(fourkt/RTB, “thermal”);
I(M, n1) <+ white_noise(fourkt/Rcontact, “thermal”);

end
endmodule

The ADMS syntax is a subset of Verilog-A. Allowed language structures are outlined in a SYNTAX-SUPPORTED file which can be downloaded from http://mot-adms.sourceforge.net. Recent news concerning the ADMS Verilog-A compiler can also be found on the ADMS Website Wiki.

### 4.9 End note

Resistive potentiometers are fundamental components in electronic system design. They deserve due attention when forming part of a circuit simulation package. This report introduces a number of basic properties of potentiometric devices and outlines how they can be accurately and efficiently simulated by Qucs. While writing this report I have tried to demonstrate how practical resistive potentiometer models can be constructed from a set of basic concepts. Qucs subcircuits and component defining equations form the fundamental tools for modelling a potentiometer. Both encourage interactive model development and the subsequent conversion of their properties into Verilog-A code. My thanks to Stefan Jahn for all his help and encouragement during the period I have been working on the potentiometer model and writing this report.
5 Verilog-A compact device models for GaAs MESFETs

5.1 Introduction

A previous Qucs Report\(^1\) described a MESFET model based on an equation defined device (EDD) representation of the level 1 Curtice model. This model evolved as a test example during the initial Qucs EDD development phase. Today the EDD model is popular amongst Qucs users as either a powerful non-linear component in it’s own right or as the basis of a component prototyping system for constructing compact Verilog-A device models, translated with ADMS to C++ code, compiled to object code and finally linked to the main body of the Qucs program code. Over the last year the Qucs development team has invested a significant amount of time improving both EDD prototyping and Verilog-A compact device/circuit model development, making the development process more transparent to anyone interested in trying their hand at model construction. One branch of the current Qucs modelling activities is concentrating on adding new models which fill in some of the gaps in the Qucs released model lists. One such model in this category is the GaAs MESFET. This report outlines the background and mathematical basis for a number of MESFET models. These have been coded in Verilog-A and tested using recent Qucs CVS code. They will be included in the next full release of Qucs.

5.2 The GaAs MESFET

The metal-semiconductor FET (MESFET) is a Schottky-barrier gate FET which is normally made from Gallium Arsenide. It is a popular device for high frequency applications because of it’s high electron mobility and usable gain at microwave frequencies. An early simulation model for the MESFET device was developed by Walter R. Curtice\(^2\) in 1980 at the RCA Laboratory in Princeton, New Jersey, USA. Since Curtice published his original MEFET model a number of authors

\(^1\)M. Brinson and S. Jahn, Qucs: Compact device- circuit macromodel specification; A Curtice level 1 MESFET model, http://qucs.sourceforge.net/docs.html

have contributed improvements to the basic model, including for example Statz et. al. (Raytheon)\(^3\) and TriQuint Semiconductor Inc.\(^4\). These models form the basis of the Qucs MESFET model described in this report.

### 5.3 The Qucs MESFET model

Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
<th>Default</th>
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<td>A/V(^2)</td>
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<td>Lambda</td>
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<td>(N)</td>
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\(^4\)For example, D.H. Smith, TOM-2: An improved Model for GaAs MESFETs, TriQuint Report, TriQuint Semiconductor, Inc Fe. 27, 1995 (11 pages).
<table>
<thead>
<tr>
<th>Name</th>
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<th>Description</th>
<th>Unit</th>
<th>Default</th>
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<td>M</td>
<td>$M$</td>
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<td>zero-bias gate-source capacitance</td>
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<tr>
<td>Cgd</td>
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<td>1p</td>
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<td>ILEVELD</td>
<td>drain-source current equation selector</td>
<td></td>
<td>3</td>
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<td>QLEVELS</td>
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</tr>
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<td>breakdown slope resistance</td>
<td>Ω</td>
<td>10</td>
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<td>Temp</td>
<td>$Temp$</td>
<td>device circuit temperature</td>
<td>°C</td>
<td>26.85</td>
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Where parameter LEVEL selects a MESFET model listed in Table 5.2.
MESFET gate current equations can be selected by setting parameters ILEVELS and ILEVELD. Table 5.3 lists the available options.
MESFET charge equations can be selected by setting parameters QLEVELS, QLEVELD and QLEVELDS. Table 5.4 lists the available options. Although it is possible to mix the five basic MESFET models with different gate current and
LEVEL  MESFET model type
1    Quadratic Curtice - basic form
2    Quadratic Curtice - basic plus subthreshold properties
3    Statz et. al. (Raytheon) - same as SPICE 3f5
4    TriQuint - TOM 1 model
5    TriQuint - TOM 2 model

Table 5.2: Qucs MESFET model types

<table>
<thead>
<tr>
<th>ILEVELS - ILEVELD</th>
<th>Gate-source current</th>
<th>Gate-drain current</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>Igs=0</td>
<td>Igd=0</td>
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<tr>
<td>1</td>
<td>Linear no reverse breakdown</td>
<td>Linear no reverse breakdown</td>
</tr>
<tr>
<td>2</td>
<td>Linear with reverse breakdown</td>
<td>Linear with reverse breakdown</td>
</tr>
<tr>
<td>3</td>
<td>Diode no reverse breakdown</td>
<td>Diode no reverse breakdown</td>
</tr>
<tr>
<td>4</td>
<td>Diode with reverse breakdown</td>
<td>Diode with reverse breakdown</td>
</tr>
</tbody>
</table>

Table 5.3: Qucs MESFET gate current model types

charge equation models the common default models are the ones listed in Table 5.5.

<table>
<thead>
<tr>
<th>QLEVELS</th>
<th>QLEVELD</th>
<th>QLEVELDS</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>Qgs=0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>Constant cap.</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>Diode</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>Statz</td>
<td>3</td>
</tr>
</tbody>
</table>

Table 5.4: Qucs MESFET charge equation types
### Table 5.5: Qucs MESET default selection parameters

<table>
<thead>
<tr>
<th>Model</th>
<th>LEVEL</th>
<th>ILEVELS</th>
<th>ILEVELD</th>
<th>QLEVELS</th>
<th>QLEVELD</th>
<th>QLEVELDS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Curtice L1</td>
<td>1</td>
<td>0 to 4</td>
<td>0 to 4</td>
<td>0 to 2</td>
<td>0 to 2</td>
<td>0 to 2</td>
</tr>
<tr>
<td>Curtice (Adv.)</td>
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<td>0 to 2</td>
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<td>Statz-Raytheon</td>
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<td>4</td>
<td>3</td>
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<td>2</td>
</tr>
<tr>
<td>TOM 1</td>
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<td>4</td>
<td>4</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>TOM 2</td>
<td>5</td>
<td>4</td>
<td>4</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

#### 5.4 The Qucs MESFET simulation model

The large signal equivalent circuit for the Qucs MESFET model is illustrated in Fig. 5.1. The currents flowing in each of the circuit branches are given by the Verilog-A code fragment shown in Fig. 5.1. The Verilog-A HDL code for the entire Qucs MESFET model is available from the Qucs CVS archive\(^5\). In order to simulate the operation of an MESFET, equations based on the physical operation of the device are required for all the current contribution components in Fig. 5.1. These equations are presented in the remaining sections of this report. Examples are also introduced to demonstrate the simulation performance of each model.

#### 5.5 MESFET gate current equations

- **ILEVELS = 0**: \( I_{gs} = 0 \) A
- **ILEVELS = 1**: if \( V(b_1) > V_{bi} \)
  \[
  I_{gs} = \frac{V(b_1) - V_{bi}}{R_f} 
  \]
  else
  \[
  I_{gs} = -Area \cdot I_{s} + GMIN \cdot V(b_1) 
  \]
- **ILEVELS = 2**: if \( V(b_1) > V_{bi} \)
  \[
  I_{gs1} = \frac{V(b_1) - V_{bi}}{R_f} 
  \]
  else
  \[
  I_{gs1} = -Area \cdot I_{s} + GMIN \cdot V(b_1) 
  \]
  if \( V(b_1) < -Bv \)
  \[
  I_{gs2} = \frac{V(b_1) - V_{bi}}{R_1} 
  \]

\(^5\)http://qucs.sourceforge.net/
\[ I_{gs} = I_{gs1} + I_{gs2} \] (5.4)

- **ILEVELS = 3:** if \( V(b1) > V_{bi} \)

\[ I_{gs} = I_{s-T2} \cdot \left\{ \text{limexp} \left( \frac{V(b1)}{N \cdot V_{t-T2}} \right) - 1.0 \right\} + GMIN \cdot V(b1) \] (5.5)

else \( I_{gs} = -I_{s-T2} + GMIN \cdot V(b1) \)

- **ILEVELS = 4:** if \( V(b1) > -5 \cdot N \cdot V_{t-T2} \)

\[ I_{gs1} = \text{Area} \cdot I_{s-T2} \cdot \left\{ \text{limexp} \left( \frac{V(b1)}{N \cdot V_{t-T2}} \right) - 1.0 \right\} + GMIN \cdot V(b1) \] (5.6)

else \( I_{gs1} = 0 \)

if \( (-Bv < V(b1)) \) and \( (V(b1) < -5 \cdot N \cdot V_{t-T2}) \)

\[ I_{gs2} = -\text{Area} \cdot I_{s-T2} + GMIN \cdot V(b1) \] (5.7)

else \( I_{gs2} = 0 \)

if \( V(b1) == -Bv \)

\[ I_{gs3} = -I_{bv} \] (5.8)

else \( I_{gs3} = 0 \)

if \( V(b1) < -Bv \)

\[ I_{gs4} = -\text{Area} \cdot I_{s-T2} \cdot \left\{ \text{limexp} \left( \frac{-(Bv + V(b1))}{V_{t-T2}} \right) - 1.0 + \frac{Bv}{V_{t-T2}} \right\} \] (5.9)

else \( I_{gs4} = 0 \)

\[ I_{gs} = I_{gs1} + I_{gs2} + I_{gs3} + I_{gs4} \] (5.10)

Where \( xx_{-T2} \) indicates the values of temperature dependent parameters at circuit temperature \( T2 \). See later sections of this report for more details. The gate to drain current equations are identical except \( I_{gs} \) is replaced by \( I_{gd} \), \( I_{gsx} \) by \( I_{gdx} \), and \( V(b1) \) by \( V(b2) \). More details can be found in the Verilog-A listing given in the Qucs CVS code held at the Qucs Sourceforge site.
5.6 MESFET charge equations QLEVELS 0 to 2

- QLEVELS = 0: [NO charge]:

\[ Qgs = 0 \]  \hspace{1cm} (5.11)

- QLEVELS = 1: [Fixed capacitor charge]

\[ Qgs = Area \cdot Cgs \cdot V(b4) \]  \hspace{1cm} (5.12)

- QLEVELS = 2: [Diode charge]

if \( V(b4) < (Fc \cdot Vbi) \)

\[ Qgs1 = \frac{Cgs \cdot T2 \cdot Vbi \cdot T2}{(1 - M)} \cdot \left\{ 1 - \left( \frac{V(b4)}{Vbi \cdot T2} \right)^{1-M} \right\} \]  \hspace{1cm} (5.13)

if \( V(b4) \geq (Fc \cdot Vbi) \)

\[ H1 = \frac{M}{2 \cdot Vbi \cdot T2} \cdot (V(b4) \cdot V(b4) - (Fc \cdot Fc \cdot Vbi \cdot T2 \cdot Vbi \cdot T2)) \]  \hspace{1cm} (5.14)

\[ Qgs2 = Cgs \cdot T2 \cdot \left[ F1 + \frac{1}{F2} \cdot \{ F3 \cdot (V(b4) - Fc \cdot Vbi \cdot T2) + H1 \} \right] \]  \hspace{1cm} (5.15)
\[ F_1 = \frac{V_{bi,T_2}}{1 - M} \cdot \left\{ 1 - (1 - Fc)^{1-M} \right\}, \quad (5.16) \]
\[ F_2 = (1 - Fc)^{1+M}, \quad (5.17) \]

and
\[ F_3 = 1 - Fc \cdot (1 + M). \quad (5.18) \]

Again \( xx_{T2} \) indicates the values of temperature dependent parameters at circuit temperature \( T_2 \). See a later section of this report for more details. The gate to drain charge equations (types 0 to 2) are identical except \( Qgs \) is replaced by \( Qgd \), \( Qgsx \) by \( Qgdx \), and \( V(b4) \) by \( V(b6) \). More details can be found in the Qucs CVS code held at the Qucs Sourceforge site.

5.7 MESFET charge equations QLEVELDS 0 to 2

- QLEVELDS = 0: [NO charge]:
  \[ Qds = 0 \quad (5.19) \]

- QLEVELDS = 1: [Fixed capacitor charge]
  \[ Qds = Area \cdot Cds \cdot V(b3) \quad (5.20) \]

- QLEVELS = 2: [Fixed capacitor plus transit charge]
  \[ Qds = Area \cdot Cds \cdot V(b3) + Tau \cdot Ids \quad (5.21) \]

5.8 Curtice hyperbolic tangent model: LEVEL = 1

If \( (V(b1) - V_{to,T2}) > 0 \)
\[ Ids = Beta_{T2} \cdot (V(b1) - V_{to,T2})^2 \cdot \left\{ 1 + Lambda \cdot V(b3) \right\} \cdot \tanh(Alpha \cdot V(b3)) \quad (5.22) \]

else \( Ids = 0 \).
Figure 5.2: Curtice LEVEL 1 DC test circuit and Ids-Vds characteristics
Figure 5.3: Curtice LEVEL 1 DC test circuit and Ids-Vgs characteristics
Figure 5.4: Curtice LEVEL 1 DC test circuit and Ig-Vgs characteristics
Figure 5.5: Curtice LEVEL 1 S parameter test circuit and characteristics
5.9 Curtice hyperbolic tangent model with subthreshold modification: LEVEL = 2

\[ \text{Ids} = \text{Beta}_T \cdot Vf^2 \cdot \{1 + \text{Lambda} \cdot V(b3)\} \cdot \text{tanh}(\text{Alpha} \cdot V(b3)) \] (5.23)

Where

\[ Vf = \frac{1}{Ah} \cdot \ln \left\{1 + \exp (Ah \cdot (V(b1) - \text{Vto}_T)) \right\} \] (5.24)

and

\[ Ah = \frac{1}{2 \cdot Nsc \cdot Vt_T} \] (5.25)

When \( V(b2) > \text{Vto}_T \), \( Vf \rightarrow V(b2) - \text{Vto}_T \). Otherwise, \( Vf \) approaches zero asymptotically. This modification to the basic Curtice model provides an improved match to channel gradual pinch-off and MESFET subthreshold conduction.
Figure 5.6: Curtice LEVEL 2 DC test circuit and Ids-Vgs characteristics illustrating subthreshold conduction modification
5.10 Statz et. al. (Raytheon) model: LEVEL = 3

if \((V(b_1) - V_{to\_T2}) > 0\)
\[\text{if } (0 < V(b_3)) \text{ and } (V(b_3) < \frac{3}{\text{Alpha}})\]
begin
\[H_1 = \frac{1 - \left(1 - \frac{\text{Alpha} \cdot V(b_3)}{3}\right)^3}{1 + B \cdot (V(b_1) - V_{to\_T2})}\] (5.26)
\[I_{ds} = \text{Beta}_{\_T2} \cdot \left\{1 + \text{Lambda} \cdot V(b_3)\right\} \cdot (V(b_1) - V_{to\_T2})^2 \cdot H_1\] (5.27)
end
\[\text{if } (V(b_3) > \frac{3}{\text{Alpha}})\]
\[I_{ds} = \frac{\text{Beta}_{\_T2} \cdot \left\{1 + \text{Lambda} \cdot V(b_3)\right\} \cdot (V(b_1) - V_{to\_T2})^2}{1 + B \cdot (V(b_1) - V_{to\_T2})}\] (5.28)
else \(I_{ds} = 0.\)

5.10.1 MESFET charge equations QLEVELS = 3 and QLEVELD = 3

QLEVELS = 3 : Statz et. al. charge equations
\[V_{max} = \min(Fc \cdot V_{bi}, V_{max})\] (5.29)
\[V_{eff1} = 0.5 \cdot \left\{V(b_4) + V(b_6) + \sqrt{(V(b_6) - V(b_4))^2 + V_{delta1}^2}\right\}\] (5.30)
\[V_{new} = 0.5 \cdot \left\{V_{eff1} + V_{to\_T2} + \sqrt{(V_{eff1} - V_{to\_T2})^2 + V_{delta2}^2}\right\}\] (5.31)
if \((V_{new} > V_{max})\)
\[Q_{gs} = C_{gs\_T2} \cdot \left\{2 \cdot V_{bi\_T2} \left(1 - \sqrt{1 - \frac{V_{max}}{V_{bi\_T2}}} + \frac{V_{new} - V_{max}}{\sqrt{1 - \frac{V_{max}}{V_{bi\_T2}}}}\right)\right\}\] (5.32)
if \((V_{new} \leq V_{max})\)
\[Q_{gs} = C_{gs\_T2} \cdot 2 \cdot V_{bi\_T2} \cdot \left\{1 - \sqrt{1 - \frac{V_{new}}{V_{bi\_T2}}}\right\}\] (5.33)
Figure 5.7: Statz et. al. LEVEL 3 DC test circuit and Ids-Vds characteristics

QLEVELD = 3 : Statz et. al. charge equations

\[ V_{eff2} = 0.5 \cdot \left\{ V(b4) + V(b6) - \sqrt{(V(b4) - V(b6))^2 + V_{delta}^2} \right\} \quad (5.34) \]

\[ Q_{ds} = C_{gd \cdot T2} \cdot V_{eff2} \quad (5.35) \]

During simulation gate charge must be partitioned between gate-source and gate-drain branches. The Qucs implementation of the Statz et. al. MESFET model uses the procedure adopted by Divehar.\(^6\)

Figure 5.8: Statz et. al. LEVEL 3 DC test circuit and Ids-Vgs characteristics
Figure 5.9: Statz et. al. LEVEL 3 DC test circuit and Ig-Vgs characteristics
Figure 5.10: Statz et. al. LEVEL 3 S parameter test circuit and characteristics
5.11 TriQuint Semiconductor TOM 1 model: 
LEVEL = 4

if \((V(b1) - V_{to_T2}) > 0\)
    if \((0 < V(b3))\) and \((V(b3) < \frac{3}{3}\))
        begin
            \[
            I_ds1 = \left\{ Beta_{-}T2 \cdot (V(b1) - V_{to_T2})^{Q_p} \right\} \cdot \left\{ 1 - \left\{ 1 - \frac{Alpha \cdot V(b3)}{3} \right\}^3 \right\}
            \]
            \[
            I_ds = \frac{I_ds1 \cdot \{1 + Lambda \cdot V(b3)\}}{1 + Delta \cdot V(b3) \cdot I_ds1}
            \] (5.36) (5.37)
        end
    if \((V(b3) > \frac{3}{3}\))
        \[
        I_ds1 = Beta_{-}T2 \cdot (V(b1) - V_{to_T2})^{Q_p}
        \] (5.38)
        \[
        I_ds = \frac{I_ds1 \cdot \{1 + Lambda \cdot V(b3)\}}{1 + Delta \cdot V(b3) \cdot I_ds1}
        \] (5.39)
else \(I_ds = 0\).
Figure 5.11: TOM1 LEVEL 4 DC test circuit and Ids-Vds characteristics

Figure 5.12: TOM1 LEVEL 4 DC test circuit and Ids-Vgs characteristics
Figure 5.13: TOM1 LEVEL 4 DC test circuit and Ig-Vgs characteristics
Figure 5.14: TOM1 LEVEL 4 S parameter test circuit and characteristics
5.12 TriQuint Semiconductor TOM 2 model: LEVEL = 5

if \((V(b1) - Vto\_T2) > 0\) begin

\[ Nst = Ng + Nd \cdot V(b3) \]  
(5.40)

if \((Nst < 1.0)Nst = 1.0\)

\[ Vst = Nst \cdot Vt\_T2 \]  
(5.41)

\[ Vg = Qp \cdot Vst \cdot \ln \left( \exp \left\{ \frac{V(b1) - Vto\_T2 + Gamma\_T2 \cdot V(b3)}{Qp \cdot Vst} \right\} + 1 \right) \]  
(5.42)

\[ Al = Alpha\_T2 \cdot V(b3) \]  
(5.43)

\[ Fd = \frac{Al}{\sqrt{1 + Al \cdot Al}} \]  
(5.44)

\[ Ids1 = Beta\_T2 \cdot Vg^{Qp} \cdot Fd \]  
(5.45)

\[ Ids = Ids1 \cdot \frac{1 + Lambda \cdot V(b3)}{1 + Delta \cdot V(b3) \cdot Ids1} \]  
(5.46)

end

else \(Ids = 0\)
Figure 5.15: TOM2 LEVEL 5 DC test circuit and Ids-Vds characteristics
Figure 5.16: TOM2 LEVEL 5 DC test circuit and Ids-Vgs characteristics
Figure 5.17: TOM2 LEVEL 5 DC test circuit and Ig-Vgs characteristics
Figure 5.18: TOM2 LEVEL 5 S parameter test circuit and characteristics
5.13 Temperature scaling relations

\[ T_1 = T_{\text{nom}} + 273.15; \]
\[ T_2 = \text{Temp} + 273.15; \]
\[ T_r = T_2 / T_1; \]
\[ \text{con1} = \text{pow}(T_r, 1.5); \]
\[ R_{g,T_2} = R_g \times (1 + R_{gTC}(T_2 - T_1)); \]
\[ R_{d,T_2} = R_d \times (1 + R_{dTC}(T_2 - T_1)); \]
\[ R_{s,T_2} = R_s \times (1 + R_{sTC}(T_2 - T_1)); \]
\[ \text{Beta}_{T_2} = \text{Area} \times \text{Beta} \times \text{pow}(1.01, \text{Betatc}(T_2 - T_1)); \]
\[ V_{t,T_2} = \$v_t; \]
\[ E_{g,T_1} = E_g - 7.02 \times 10^{-4} \times T_1 \times T_1 / (1108 + T_1); \]
\[ E_{g,T_2} = E_g - 7.02 \times 10^{-4} \times T_2 \times T_2 / (1108 + T_2); \]
\[ V_{bi,T_2} = (T_r \times V_{bi}) - 2 \times V_{t,T_2} \times \ln(\text{con1}) - (T_r \times E_{g,T_1} - E_{g,T_2}); \]
\[ I_{s,T_2} = \text{Area} \times I_s \times \text{pow}(T_r, (X_t/N)) \times \text{limexp}(-('P_Q \times E_{g,T_1} \times (1 - T_r) / ('P_K \times T_2)); \]
\[ C_{gs,T_2} = \text{Area} \times C_{gs} \times (1 + M \times (400 \times 10^{-6}(T_2 - T_1) - (V_{bi,T_2} - V_{bi}) / V_{bi}); \]
\[ C_{gd,T_2} = \text{Area} \times C_{gd} \times (1 + M \times (400 \times 10^{-6}(T_2 - T_1) - (V_{bi,T_2} - V_{bi}) / V_{bi}); \]
\[ V_{to,T_2} = V_{to} + V_{to TC}(T_2 - T_1); \]
\[ \Gamma_{T_2} = \Gamma \times (1 + \text{Gammatc}(T_2 - T_1)); \]
\[ \alpha_{T_2} = \alpha \times (\text{pow}(1.01, \text{Alphatc}(T_2 - T_1))); \]

5.14 MESFET noise

5.14.1 Main components

- Thermal noise: generated by resistors \( R_g, R_d \) and \( R_s \).
- Gate noise: Mainly channel noise induced in the gate (via the channel to gate capacitance) The resulting noise is amplified by the MESFET. The capacitive coupling causes the gate noise to have a power spectral density proportional to frequency.
- Flicker noise: Due to random carrier generation-recombination in the lattice imperfections or contaminating impurities. Flicker noise power has a \( 1 / f^n \) behavior, with \( n \approx 1 \).

A typical plot of GaAs MESFET \( I_{ds} \) noise current is shown in Fig. 5.19, where
Figure 5.19: Typical GaAS MESFET $I_{ds}$ noise characteristic

The device drain to source noise current is given by

$$ I_{dsn} = \text{channel-thermal-noise-current} + \text{flicker-noise-current} \quad (5.47) $$

To a first approximation:

- **Channel-thermal-noise-current**

  $$\text{Channel-thermal-noise-current} = \sqrt{\frac{8 \cdot K \cdot T}{3} \cdot gm \cdot \left\{ \frac{1 + \alpha + \alpha^2}{1 + \alpha} \right\} \cdot G_d s n o i}$$
  
  Where $gm = \frac{\partial I_{ds}}{\partial V_{gs}}$,
  
  and $\alpha = 1 - \frac{V_{ds}}{V_{gs} - V_{to}}$, when $V_{ds} < \frac{3}{\text{Alpha}}$ – Linear region of operation
  
  Or $\alpha = 0$, when $V_{ds} \geq \frac{3}{\text{Alpha}}$ – Saturation region of operation

- **Flicker-noise-current**

  $$\text{Flicker-noise-current} = \sqrt{K_f \cdot I_{ds}^{\alpha_f}}$$

- **Resister thermal noise equations**

  $$IR_{gn} = \sqrt{\frac{4 \cdot K \cdot T}{R_g}}, \quad IR_{dn} = \sqrt{\frac{4 \cdot K \cdot T}{R_d}},$$
  
  and $IR_{sn} = \sqrt{\frac{4 \cdot K \cdot T}{R_s}}$
5.14.2 MESFET equivalent circuit with noise current components

5.14.3 Curtice hyperbolic tangent model: LEVEL = 1 or 2:
Noise equations

1. Verilog-A equations

```verilog
fourkt = 4.0*`P_K*T2;
gm = 2*Beta_T2*(V(b1)-Vto_T2)*(1+Lambda*V(b3))*tanh(Alpha_T2*V(b3));
if ( V(b3) < 3/Alpha ) begin
    An = 1-V(b3)/(V(b1)-Vto_T2);
    thermal_pwr = (8*`P_K*T2*gm/3)*((1+An+An*An)/(1+An))*Gdsnoi;
end else
    thermal_pwr = (8*`P_K*T2*gm/3)*Gdsnoi;
I(b3) <+ white_noise(thermal_pwr,"thermal");
I(b3) <+ flicker_noise(flicker_pwr,1.0,"flicker");
end
I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");
```

7Tsivids and Yanis, Operation and modeling of the MOS transistor, McGraw-Hill 1987, p340
2. Typical noise simulation results

Figure 5.21: Typical LEVEL 1 (or 2) GaAS MESFET Ids noise characteristic

5.14.4 Statz et. al. (Raytheon) model: LEVEL = 3: Noise equations

1. Verilog-A equations
if ( V(b3) < 3/Alpha )begin
H1=((1-(1-(Alpha*V(b3))/3))/(1+B*(V(b1)-Vto_T2));
gm=2*Beta_T2*(V(b1)-Vto_T2)*(1+Lambda*V(b3))*H1+(Beta_T2*
(1+Lambda*V(b3))*pow((V(b1)-Vto_T2),2))*B*H1/(1+B*(V(b1)-Vto_T2));
An=1-V(b3)/(V(b1)-Vto_T2);
thermal_pwr= (8*’P_K*T2*gm/3)*((1+An+An*An)/(1+An))*Gdsnoi;
end
else begin
  gm=2*Beta_T2*(V(b1)-Vto_T2)*(1+Lambda*V(b3))/(1+B*(V(b1)-Vto_T2))+
  (Beta_T2*(1+Lambda*V(b3))*pow((V(b1)-Vto_T2),2))
  *B/pow( (1+B*(V(b1)-Vto_T2)),2);
  thermal_pwr=(8*’P_K*T2*gm/3)*Gdsnoi;
end
I(b3) <+ white_noise(thermal_pwr, "thermal");
flicker_pwr = Kf*pow(Ids,Af);
I(b3) <+ flicker_noise(flicker_pwr,1.0, "flicker");
I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");
I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal");
I(b9) <+ white_noise(Area*fourkt/Rs_T2, "thermal");

2. Typical noise simulation results

5.14.5 TriQuint Semiconductor TOM 1 model: LEVEL = 4:
Noise equations

1. Verilog-A equations

if ( V(b3) < 3/Alpha )begin
Ids1=(Beta_T2*pow( (V(b1)-Vto_T2), Qp ))*(1-pow( (1-Alpha*V(b3)/3), 3));
gm1=Qp*Beta_T2*pow( (V(b1)-Vto_T2), Qp-1 )*(1-1-pow(Alpha*V(b3)/3, 3));
gm=gm1*(1+Lambda*V(b3))/((1+Delta*V(b3)*Ids1))*(1+(Delta*V(b3)*Ids1)/
(1+Delta*V(b3)*Ids1));
An=1-V(b3)/(V(b1)-Vto_T2);
thermal_pwr= (8*’P_K*T2*gm/3)*((1+An+An*An)/(1+An))*Gdsnoi;
end
else begin
  Ids1=(Beta_T2*pow( (V(b1)-Vto_T2), Qp ));
gm1=Qp*Beta_T2*pow( (V(b1)-Vto_T2), Qp-1 );
gm=(gm1*(1+Lambda*V(b3))/((1+Delta*V(b1)*Ids1))*(1+(Delta*V(b3)*Ids1)/
(1+Delta*V(b3)*Ids1));
  thermal_pwr=(8*’P_K*T2*gm/3)*Gdsnoi;
end
Figure 5.22: Typical LEVEL 3 GaAS MESFET Ids noise characteristic

end
I(b3) <+ white_noise(thermal_pwr, "thermal");
flicker_pwr = Kf*pm(Ids,Af);
I(b3) <+ flicker_noise(flicker_pwr,1.0, "flicker");
I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");
I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal");
I(b9) <+ white_noise(Area*fourkt/Rs_T2, "thermal");

2. Typical noise simulation results

5.14.6 TriQuint Semiconductor TOM 2 model: LEVEL = 5

1. Verilog-A equations

    if ( V(b3) < 3/Alpha )begin
        Nst=Ng+Nd*V(b3);
        if ( Nst < 1.0) Nst=1.0;
        Vst=Nst*Vt_T2;
    end

Figure 5.23: Typical LEVEL 4 GaAS MESFET Ids noise characteristic

\[
V_g = Q_p \times V_{st} \ln \left( \exp \left( \frac{(V(b1)-V_{to_T2}+\Gamma_{T2} \times V(b3))}{Q_p \times V_{st}} \right) + 1 \right)
\]

\[
A_l = \alpha_{T2} \times V(b3)
\]

\[
F_d = \frac{A_l}{\sqrt{1 + (A_l \times A_l)}}
\]

\[
I_{ds1} = \beta_{T2} \times (V_g)^{Q_p} \times F_d
\]

\[
g_m1 = \frac{I_{ds1}}{V_g} \times Q_p \times \frac{1}{\exp \left(-\frac{(V(b1)-V_{to_T2}+\Delta \times V(b3))}{Q_p \times V_{st}} \right) + 1}
\]

\[
g_m = \frac{g_m1}{(1 + \Delta \times V(b3) \times I_{ds1})^2}
\]

\[
A_n = 1 - \frac{V(b3)}{V(b1)-V_{to_T2}}
\]

\[
\text{thermal_pwr} = \left( 8 \times P_K \times T_2 \times g_m / 3 \right) \times \left( (1 + A_n + A_n \times A_n) / (1 + A_n) \right) \times G_{ds\text{noi}}
\]

end

else begin

\[
N_{st} = N_g + N_d \times V(b3)
\]

if ( N_{st} < 1.0) N_{st} = 1.0;

\[
V_{st} = N_{st} \times V_{t_{T2}}
\]

\[
V_g = Q_p \times V_{st} \ln \left( \exp \left( \frac{(V(b1)-V_{to_T2}+\Gamma_{T2} \times V(b3))}{Q_p \times V_{st}} \right) + 1 \right)
\]

\[
A_l = \alpha_{T2} \times V(b3)
\]

\[
F_d = \frac{A_l}{\sqrt{1 + (A_l \times A_l)}}
\]

\[
I_{ds1} = \beta_{T2} \times (V_g)^{Q_p} \times F_d
\]

\[
g_m1 = \frac{I_{ds1}}{V_g} \times Q_p \times \frac{1}{\exp \left(-\frac{(V(b1)-V_{to_T2}+\Delta \times V(b3))}{Q_p \times V_{st}} \right) + 1}
\]

\[
g_m = \frac{g_m1}{(1 + \Delta \times V(b3) \times I_{ds1})^2}
\]

\[
\text{thermal_pwr} = \left( 8 \times P_K \times T_2 \times g_m / 3 \right) \times G_{ds\text{noi}}
\]

end

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I(b3) <+ white_noise(thermal_pwr, "thermal");
flicker_pwr = Kf*pow(Ids,Af);
I(b3) <+ flicker_noise(flicker_pwr,1.0, "flicker");
I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");
I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal");
I(b9) <+ white_noise(Area*fourkt/Rs_T2, "thermal");

2. Typical noise simulation results

Figure 5.24: Typical LEVEL 5 GaAS MESFET Ids noise characteristic

5.15 Adding external passive components to the MESFET models

The Curtice model outlined in the first Qucs report on MESFETs included lead inductance in each of the device signal paths. These inductances were not included in the Verilog-A models described in this report, mainly to simplify the model code. If required they can be added as external components. The test circuit shown in Fig. 5.25 indicates how this can be done and illustrates the effect such components have on the Curtice S parameter characteristics.
Figure 5.25: S parameter simulated characteristics for test circuit shown in Fig. 5.5 that has external inductance added
5.16 End note

MESFETs are important high frequency devices which have been missing from the range of active component models supplied with Qucs. While developing the models described in this report I have attempted to make them as flexible as possible so as to allow users the opportunity to select which model, or indeed the make-up of the components of a model, they would like to try for a specific simulation. The work described in this report is very much work in progress, mainly because there are a number of other published MESFET models that have not been included. My intention has simply been to provide a number of practical models which were not previously available to Qucs users. Also knowing that many Qucs users have an interest in high frequency circuit design and simulation, the work would be of direct relevance to making Qucs more “universal”. The procedures employed for model development are another example of the work being undertaken by the Qucs team in response to Qucs being adopted by the wider modelling community as part of the Verilog-A compact device standardization project. Overall the simulation results from the models described here show a high degree of consistency from DC to the high frequency S parameter domain. The noise results are particularly interesting as they are based on mix of available theories and extensions introduced especially for Qucs. Some readers will probably have spotted one area where there appears to be differences in the simulation results from the different models; look at the S[1,2] and S[2,1] characterstics for each model. Here there are noticeable difference which are possibly due to the lack of symmetry in some of the model charge equations? MESFET modelling is a complex subject, suggesting that there are likely to be errors /bugs in the models. If you find an error/bug please inform the Qucs development team so that we can correct problems as they are found. In the future, particularly if the response to this group of models is positive, I will attempt to add more MESFET models to Qucs. Once again a special thanks to Stefan Jahn for all his help and encouragement over the period that I have been developing the Qucs MESFET models and writing the report which outlines their physical and mathematical fundamentals.
6 Verilog-A implementation of the EKV v2.6 long and short channel MOSFET models

6.1 Introduction

This report presents the background to the Qucs implementation of the EKV 2.6 long and short channel MOSFET models. During 2007 the Qucs development team employed the EKV v2.6 MOSFET model as a test case while developing the Qucs non-linear equation defined devices (EDD)\(^1\). More recently complete implementations of the long and short channel EKV v2.6 models have been developed using the Qucs Verilog-A compact device modelling route. This work forms part of the Verilog-A compact device modelling standardisation initiative\(^2\). The EKV v2.6 MOSFET model is a physics based model which has been placed in the public domain by its developers. It is ideal for analogue circuit simulation of submicron CMOS circuits. Since the models introduction and development between 1997 and 1999 it has been widely used in industry and by academic circuit design groups. Today the EKV v2.6 model is available with most of the major commercial simulators and a growing number of GPL simulators. The Verilog-A code for the Qucs ADMS\(^3\) compiled version of the EKV v2.6 model is given in an appendix to this report.

6.2 Effects modelled

The EKV v2.6 MOSFET model includes the following effects:

\(^1\)An example EDD macromodel of the short channel EKV 2.6 model can be found at http://qucs.sourceforge.net/.


Basic geometrical and process related features dependent on oxide thickness, junction depth, effective channel length and width

- Effects of doping profile
- Modelling of weak, moderate and strong inversion behaviour
- Modelling of mobility effects due to vertical and lateral fields, velocity saturation
- Short channel effects including channel-length modulation, source and drain charge-sharing and reverse channel effect
- Modelling of substrate current due to impact ionization
- Thermal and flicker noise
- First order non-quasistatic model for the transconductances
- Short-distance geometry and bias dependent device matching

The Qucs implementation of the short channel EKV v2.6 model includes nearly all the features listed above. A simpler long channel version of the model is also available for those simulations that do not require short channel effects. Both nMOS and pMOS devices have been implemented. No attempt is made in this report to describe the physics of the EKV v2.6 model. Readers who are interested in learning more about the background to the model, its physics and function should consult the following references:


This first release of the Qucs implementation of the EKV v2.6 MOSFET model does not include the first-order non-quasistatic model for transconductances.
6.3 The Qucs long channel EKV v2.6 model

A basic DC model for the long channel nMOS EKV v2.6 model is given at the EKV Compact MOSFET model website\(^5\). Unfortunately, this model is only of limited practical use due to its restricted modelling features\(^6\). It does however, provide a very good introduction to compact device modelling using the Verilog-A hardware description language. Readers who are unfamiliar with the Verilog-A hardware description language should consult the following references:


The equivalent circuit of the Qucs EKV long channel n type MOSFET model is shown in Fig. 6.1. In this model the inner section, enclosed with the red dotted box, represents the fundamental intrinsic EKV v2.6 elements. The remaining components model extrinsic elements which represent the physical components connecting the intrinsic MOSFET model to its external signal pins. In the Qucs implementation of the EKV v2.6 long channel MOSFET model the drain to source

\(^6\)No dynamic, noise or temperature effects.
Intrinsic model

Figure 6.1: Equivalent circuit for the Qucs EKV v2.6 long channel nMOS model

DC current Ids is represented by the equations listed in a later section of the report, capacitors $C_{gdi}$, $C_{gsi}$, $C_{dbi}$ and $C_{sbi}$ are intrinsic components derived from the charge-based EKV equations, capacitors $C_{gdo}$, $C_{gso}$ and $C_{gbo}$ represent external overlap elements, the two diodes model the drain to channel and source to channel junctions (including diode capacitance) and resistors $R_{Deff}$ and $R_{Seff}$ model series connection resistors in the drain and source signal paths respectively.

6.3.1 Long channel model parameters (LEVEL = 1)

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<td>$R_{sc}$</td>
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<td>$F$</td>
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<td>$A$</td>
<td>1e-3</td>
<td>1e-3</td>
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6.3.2 Fundamental long channel DC model equations (LEVEL = 1)

\[
V_g = V(Gate) - V(Bulk)
\]

\[
V_s = V(Source) - V(Bulk)
\]

\[
V_d = V(Drain) - V(Bulk)
\]

\[
VG' = V_g - V_{to} + \Phi + \Gamma \cdot \sqrt{\Phi}
\]

\[
V_p = VG' - \Phi - \Gamma \cdot \left[ \ln \left( 1 + \lim_{x \to 0} \exp \left( \frac{X_1}{2} \right) \right) \right]^{\frac{1}{2}}
\]

\[
X_1 = \frac{V_p - V_s}{Vt}
\]

\[
X_2 = \frac{V_p - V_d}{Vt}
\]

\[
\beta = K_p \cdot \frac{L}{1 + \Theta \cdot V_p}
\]

\[
\text{Ispecific} = 2 \cdot n \cdot \beta \cdot Vt^2
\]

\[
\text{Ids} = \text{Ispecific} \cdot (I_f - I_r)
\]

Where \( VG' \) is the effective gate voltage, \( V_p \) is the pinch-off voltage, \( n \) is the slope factor, \( \beta \) is a transconductance parameter, \( \text{Ispecific} \) is the specific current, \( I_f \) is the forward current, \( I_r \) is the reverse current, \( Vt \) is the thermal voltage at the device temperature, and \( \text{Ids} \) is the drain to source current. EKV v2.6 equation numbers are given in “< >” brackets at the left-hand side of each equation. Typical plots of \( \text{Ids} \) against \( Vds \) for both the nMOS and pMOS long channel devices are given in Figure 6.2.
Figure 6.2: Ids versus Vds plots for the Qucs EKV v2.6 long channel nMOS and pMOS models
6.4 Testing model performance

Implementing advanced component models like the EKV v2.6 MOSFET model is a complex process, involving the translation of a set of equations into the Verilog-A hardware design language, conversion of the Verilog-A code into C++ code via the ADMS compiler, and finally compiling and linking the model code with the main body of Qucs code. At all stages in the process accuracy becomes an important issue. This section of the Qucs EKV v2.6 report introduces a number of test simulations which were used during the model development cycle to check the performance of the Qucs EKV v2.6 implementation. The tests also demonstrate how a circuit simulator can be used to extract model parameters. The values of which help to confirm correct model operation.

6.4.1 Extraction of Ispec

When a MOS transistor is operating in the saturation region, reverse current \( I_r \) approaches zero and the drain to source current is approximated by

\[
    I_{ds} = I_{specific} \cdot I_f = I_{specific} \cdot \left[ \ln \left( 1 + \lim_{x \to V_t} \left( \frac{V_p - V_s}{2 \cdot V_t} \right) \right) \right]^2
\]  

(6.1)

In saturation \( \lim_{x \to V_t} \left( \frac{V_p - V_s}{2 \cdot V_t} \right) \gg 1 \), yielding

\[
    \sqrt{I_{ds}} = \sqrt{\frac{I_{specific}}{2 \cdot V_t^2}} \cdot (V_p - V_s)
\]  

(6.2)

Hence

\[
    \frac{\partial (\sqrt{I_{ds}})}{\partial V_s} = -\sqrt{\frac{I_{specific}}{2 \cdot V_t^2}} = -slope
\]  

(6.3)

Or

\[
    I_{specific} = 2 \cdot slope^2 \cdot V_t^2
\]  

(6.4)

Figure 6.3 shows a typical test circuit configuration for measuring and simulating \( I_{ds} \) with varying \( V_s \). Qucs post-simulation functions in equation block Eqn1 are used to calculate the value for \( I_{specific} \). The value of \( I_{specific} \) for the nMOS transistor with the parameters given in Fig. 6.3 is 3.95e-8 A. Figure 6.4 illustrates a test circuit for measuring \( V_p \) with the transistor in saturation. In this circuit \( I_s = I_{specific} \) and the threshold voltage corresponds to \( V_g \) when \( V_p = 0V \). Notice also that \( n = \partial V_g / \partial V_p \). In Fig. 6.4 Qucs post-simulation processing functions are also used to generate data for \( V_p, V_Gprime \) and \( n \). The value of the threshold voltage for the device shown in Fig. 6.4 is 0.6V. At this voltage \( n = 1.37 \). The two test configurations illustrated in Figs. 6.3 and 6.4 go some way to confirming
that the Qucs implementation of the EKV v2.6 long channel model is functioning correctly.

### 6.4.2 Extraction of model intrinsic capacitance

The Qucs implementation of the EKV v2.6 MOSFET model uses the charge-based model for transcapacitances. This model ensures charge-conservation during transient analysis. Both the long channel and short channel versions employ the quasi-static charge-based model. The EKV v2.6 charge equations for the long channel intrinsic device are:

\[
nq = 1 + \frac{\Gamma}{2 \cdot \sqrt{V_p + \Phi_t + 1e - 6}}
\]

\[
X_f = \sqrt{\frac{1}{4} + I_f}
\]

\[
X_r = \sqrt{\frac{1}{4} + I_r}
\]

\[
q_D = -nq \cdot \left\{ \frac{4}{15} \cdot \frac{3 \cdot X_r^3 + 6 \cdot X_r^2 \cdot X_f + 4 \cdot X_r \cdot X_f^2 + 2 \cdot X_f^3}{(X_f + X_r)^2} - \frac{1}{2} \right\}
\]

\[
q_S = -nq \cdot \left\{ \frac{4}{15} \cdot \frac{3 \cdot X_f^3 + 6 \cdot X_f^2 \cdot X_r + 4 \cdot X_f \cdot X_r^2 + 2 \cdot X_r^3}{(X_f + X_r)^2} - \frac{1}{2} \right\}
\]

\[
q_I = q_S + q_D = -nq \cdot \left\{ \frac{4}{3} \cdot \frac{3 \cdot X_f^3 + X_r \cdot X_f + X_r^2}{X_f + X_r} - 1 \right\}
\]

\[
q_B = -\Gamma \cdot \sqrt{V_p + \Phi_t + 1e - 6} \cdot \frac{1}{V_t} - \left( \frac{nq - 1}{nq} \right) \cdot q_I \quad \forall (V_G > 0)
\]

\[
q_B = -V_G \cdot \frac{1}{V_t} \quad \forall (V_G <= 0)
\]

\[
q_G = -q_I - q_B
\]

\[
COX = C_{ox} \cdot N_p \cdot W_{eff} \cdot N_s \cdot L_{eff}
\]
Figure 6.3: Ispecific extraction test circuit and post simulation data processing results
Figure 6.4: Vp extraction test circuit and post simulation data processing results
\[ Q(I, B, D, S, G) = COX \cdot Vt \cdot q(I, B, D, S, G) \quad (6.15) \]

The first release of the Qucs EKV v2.6 MOSFET model assumes that the gate and bulk charge is partitioned between the drain and source in equal ratio\(^7\). Fifty percent charge portioning yields the following \( I_{ds} \) current contributions:

\[ I(\text{Gate, Source\_int}) < +0.5 \cdot p_{n\_MOS} \cdot ddt(QG) \quad (6.16) \]

\[ I(\text{Gate, Drain\_int}) < +0.5 \cdot p_{n\_MOS} \cdot ddt(QG) \quad (6.17) \]

\[ I(\text{Source\_int, Bulk}) < +0.5 \cdot p_{n\_MOS} \cdot ddt(QB) \quad (6.18) \]

\[ I(\text{drain\_int, Bulk}) < +0.5 \cdot p_{n\_MOS} \cdot ddt(QB) \quad (6.19) \]

Where \( p_{n\_MOS} = 1 \) for nMOS devices or -1 for pMOS devices. Charge associated with the extrinsic overlap capacitors, \( C_{gs0}, C_{gd0} \) and \( C_{gb0} \), is represented in the Qucs EKV v2.6 implementation by the following equations:

\[ Q_{gs0} = C_{gs0} \cdot W_{eff} \cdot Np \cdot (V_G - V_S) \quad (6.20) \]

\[ Q_{gd0} = C_{gd0} \cdot W_{eff} \cdot Np \cdot (V_G - V_D) \quad (6.21) \]

\[ Q_{gb0} = C_{gb0} \cdot L_{eff} \cdot Np \cdot V_B \quad (6.22) \]

The drain to bulk and source to bulk diodes also introduce additional components in the extrinsic capacitance model. The default value of \( C_{j0} \) being set at 300fF.

Analysis of the \( y \)-parameters\(^8\) for the EKV v2.6 equivalent circuit shown in the test circuit illustrated in Fig. 6.5 yields

\[ y_{11} = \frac{j \cdot \omega \cdot C_g}{1 + \omega^2 \cdot (R_{gn} \cdot C_g)^2} \quad (6.23) \]

\(^7\)For an example of this type of charge partitioning see F. Pregaldiny et. al., An analytic quantum model for the surface potential of deep-submicron MOSFETS, 10th International Conference, MIXDES 2003, Lodz, Poland, 26-28 June 2003.

\(^8\)A more detailed analysis of the EKV v2.6 \( y \)-parameters can be found in F. Krummenacher et. al., HF MOSET MODEL parameter extraction, European Project No. 25710, Deliverable D2.3, July 28, 2000.
Or
\[ y_{11} \cong \omega^2 \cdot Rg \cdot C_g^2 + j \cdot \omega \cdot C_g, \quad \text{when } \omega \cdot Rg \cdot C_g << 1. \] (6.24)

Hence, \( C_g = \text{imag}(y_{11}/\omega) \) and \( Rgn = \text{real}(y_{11}/(\omega^2 \cdot C_g^2)) \), where \( \omega = 2 \cdot \pi \cdot f \), and \( f \) is the frequency of y-parameter measurement, \( Rg \) is a series extrinsic gate resistance and \( C_g \cong C_{gs} + C_{gd} + C_{gb} \). With equal partitioning of the intrinsic gate charge \( C_{gb} \) approximates to zero and \( C_g \cong C_{gs} + C_{gd} \). The data illustrated in Figures 6.5 and 6.6 shows two features which are worth commenting on; firstly the values of \( C_g \) are very much in line with simple hand calculations (for example in the case of the nMOS device \( C_g(\text{max}) = W \cdot L \cdot \text{Cox} = 10e-6 \cdot 10e-6 \cdot 3.45e-3 = 3.45e-13 \text{F} \)) and secondly both sets of simulation data indicate the correct values for the nMOS and pMOS threshold voltages (for example -0.55 V for the pMOS device and 0.6 V for the nMOS device), reinforcing confidence in the EKV v2.6 model implementation.

### 6.4.3 Extraction of extrinsic diode capacitance and drain resistance

The extrinsic section of the EKV v2.6 model includes diodes which in turn are modelled by conventional DC characteristics and parallel capacitance. This capacitance is represented by depletion layer capacitance in the diode reverse bias region of operation. In the diode forward bias section of the I-V characteristic diffusion capacitance dominates. Figure 6.7 illustrates a test circuit that allows the diode capacitance to be extracted as a function of \( V_{ds} \). In Fig. 6.7 the nMOS device is turned off and the drain to bulk diode reverse biased. Simple analysis indicates that
\[ y_{11} \cong \omega^2 \cdot R_{Deff} \cdot C_d^2 + j \cdot \omega \cdot C_d, \quad \text{when } \omega \cdot R_{Deff} \cdot C_d << 1. \] (6.25)

Hence, \( C_d = \text{imag}(y_{11}/\omega) \) and \( R_{deff} = \text{real}(y_{11}/(\omega^2 \cdot C_d^2)) \), where \( \omega = 2 \cdot \pi \cdot f \), \( f \) is the frequency of y-parameter measurement, and \( C_d \) is the diode capacitance. The data shown in Fig. 6.7 indicate good agreement with the expected values for \( C_d \) and \( R_{deff} \); which are expected to be \( C_d = 300 \text{ff} \) at \( V_{ds} = 0 \text{V} \), and \( R_{deff} = 46 \Omega \).

### 6.4.4 Simulating EKV v2.6 MOSFET noise

The EKV v2.6 intrinsic device noise is modelled by a noise current source connected between the internal drain and source terminals. The noise current source \( I_{dsn} \), see Fig. 6.1, is composed of a thermal noise component and a flicker noise component. The Power Spectral Density (\( S_{PSD} \)) of these components are given by:
Figure 6.5: $y_{11}$ test circuit and values of $C_g$ for the long channel EKV v2.6 nMOS model
Figure 6.6: $y_{11}$ test circuit and values of Cg for the long channel EKV v2.6 pMOS model
Figure 6.7: Test circuit for extracting EKV v2.6 extrinsic diode capacitance
\[ S_{PSD} = S_{thermal} + S_{flicker} \]  

(6.26)

Where

- Thermal noise

\[ S_{thermal} = 4 \cdot k \cdot T \cdot \beta \cdot | qI | \]  

(6.27)

- Flicker noise

\[ S_{flicker} = \frac{K F \cdot g_{mg}^2}{N p \cdot W_{eff} \cdot N s \cdot L_{eff} \cdot C_{ox} \cdot f_{Af}}, \]  

(6.28)

\[ g_{mg} = \frac{\partial I_d}{\partial V_{gs}} = \beta \cdot V_t \cdot \left( \sqrt{\frac{4 \cdot I_f \cdot I_{specific}}{I_{specific}} + 1} - \sqrt{\frac{4 \cdot I_r \cdot I_{specific}}{I_{specific}} + 1} \right) \]  

(6.29)

Where \( \beta \) is a transconductance factor, \( qI = qD + qS \), and the other symbols are defined in the EKV v2.6 long channel parameter list or have their usual meaning.

Noise has been implemented in both the Qucs long channel and short channel EKV v2.6 models. In addition to the intrinsic device noise the Qucs EKV v2.6 model includes the thermal noise components for both extrinsic resistors \( R_{Deff} \) and \( R_{Seff} \). Figure 6.8 presents a typical noise test circuit and simulated noise currents. In Figure 6.8 four nMOS devices are biased under different DC conditions and their noise current simulated for a range of \( W \) values between 1e-6 m and 100e-6 m. The first three devices include both thermal and flicker noise components (\( KF = 1e-27 \)) while the fourth device has it’s flicker component set to zero. The resulting current noise curves clearly demonstrate the effect of summing intrinsic thermal and flicker components on the overall performance of the EKV v2.6 noise model.
Figure 6.8: Test circuit for simulating EKV v2.6 noise: $\text{Ids}$.in blue curve, $\text{Ids1}$.in red curve, $\text{Ids2}$.in black curve and $\text{Ids3}$.in green curve
6.5 The Qucs short channel EKV v2.6 model

The Qucs implementation of the short short channel EKV v2.6 MOSFET model contains all the features implemented in the long channel version of the model plus a number of characteristics specific to short channel operation. However, the short channel version of the model does not use parameter \( \Theta \). Parameter LEVEL set to 2 selects the short channel model. Both pMOS and nMOS versions of the model are available for both long and short channel implementations. The entire short channel EKV v2.6 MOSFET model is described by roughly 94 equations. Readers who are interested in the mathematics of the model should consult “The EPFL-EKV MOSFET Model Equations for Simulation” publication cited in previous text. Appendix A lists the complete Verilog-A code for the first release of the Qucs EKV v2.6 MOSFET models. Additional Verilog-A code has been added to the model equation code to (1) allow interchange of the drain and source terminals, and (2) select nMOS or pMOS devices.

6.5.1 Short channel model parameters (LEVEL = 2)

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<th>Symbol</th>
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<td>( \Omega/square )</td>
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<td>( R_{sc} )</td>
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<td>( \Omega )</td>
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<td>( 1.5e - 10 )</td>
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<td>( 4e - 10 )</td>
</tr>
<tr>
<td>N</td>
<td>( N )</td>
<td>diode emission coefficient</td>
<td></td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>Is</td>
<td>( I_s )</td>
<td>leakage current</td>
<td>( A )</td>
<td>( 1e - 1 )</td>
<td>( 1e - 14 )</td>
</tr>
</tbody>
</table>
### 6.5.2 Simulating short channel charge sharing effects

A simple test circuit for demonstrating the effects of charge sharing is given in Figure 6.9. With charge sharing disabled, by setting Weta and Leta to zero, the magnitude and slope of the $I_{ds}$ vs. $V_{ds}$ curve shows a marked difference to that where charge sharing is enabled. One point to note with this test: charge sharing in short channel devices significantly reduces the device output resistance which could have, of course, important consequences on circuit performance.
Figure 6.9: Test circuit for simulating EKV v2.6 charge sharing effects in short channel devices: $I_d$ blue curve; NO charge sharing ($W_{eta} = 0.0$, $L_{eta} = 0.0$), $I_d$ red curve; charge sharing ($W_{eta} = 0.05$, $L_{eta} = 0.28$)
6.6 End note

This report outlines some of the background to the Qucs implementation of the EKV v2.6 MOSFET model. A series of test results demonstrate a range of results that have been achieved with this new Qucs compact device model. Although the test results give data similar to what is expected in all cases it must be stressed that this is the first release of this MOSFET model and as such it will probably contain bugs. A great deal of work has gone into providing this new Qucs model. However, all the effort has been worthwhile because for the first time Qucs now has a submicron MOSFET model. Please use the model and report bugs to the Qucs development team. Much work still remains to be done in the development of MOSFET models for Qucs. In future releases both bug fixes and new models are likely to feature strongly. Once again I would like to thank Stefan Jahn and Władysław Grabiński (of MOS-AK) for their encouragement and support during the period I have been working on developing the Qucs implementation of the EKV v2.6 model and writing this report.

6.7 Qucs Verilog-A code for the EKV v2.6 MOSFET model

6.7.1 nMOS: EKV equation numbers are given on the right-hand side of code lines

```verbatim
// Qucs EPFL–EKV 2.6 nMOS model:
// The structure and theoretical background to the EKV 2.6
// Verilog–a model is presented in the Qucs EPFL–EKV 2.6 report.
// Typical parameters are for 0.5um CMOS (C) EPFL–LEG 1999.
// Geometry range: Short channel W >= 0.8um, L >= 0.5um
// Long channel W >= 2um, L >= 2um
// Voltage range: |Vgb| < 3.3V, |Vdb| < 3.3V, |Vsb| < 2V
// This is free software; you can redistribute it and/or modify
// it under the terms of the GNU General Public License as published by
// the Free Software Foundation; either version 2, or (at your option)
// any later version.
// Copyright (C), Mike Brinson, mbrin72043@yahoo.co.uk, May 2008.
#include "disciplines.vams"
#include "constants.vams"

module EKV26nMOS (Drain, Gate, Source, Bulk);
inout Drain, Gate, Source, Bulk;
electrical Drain, Gate, Source, Bulk;
// Internal nodes
electrical Drain_int, Source_int;
```
`define attr(txt) (*txt*)

// Device dimension parameters
parameter real LEVEL = 1 from [1 : 2];
  'attr(info="long/short")
parameter real L = 0.5e-6 from [0.0 : inf]
  'attr(info="length" unit = "m")
parameter real W = 10e-6 from [0.0 : inf]
  'attr(info="Width" unit = "m")
parameter real Np = 1.0 from [1.0 : inf]
  'attr(info="parallel multiple device number")
parameter real Ns = 1.0 from [1.0 : inf]
  'attr(info="series multiple device number")

// Process parameters
parameter real Cox = 3.45e-3 from [0 : inf]
  'attr(info="gate oxide capacitance per unit area" unit = "F/m**2")
parameter real Xj = 0.15e-6 from [0.01e-6 : 1.0e-6]
  'attr(info="metallurgical junction depth" unit = "m")
parameter real Dw = -0.02e-6 from [-inf : 0.0]
  'attr(info="channel width correction" unit = "m")
parameter real Dl = -0.05e-6 from [-inf : 0.0]
  'attr(info="channel length correction" unit = "m")

// Basic intrinsic model parameters
parameter real Vto = 0.6 from [1e-6 : 2.0]
  'attr(info="long channel threshold voltage" unit="V")
parameter real Gamma = 0.71 from [0.0 : 2.0]
  'attr(info="body effect parameter" unit = "V**(1/2)")
parameter real Phi = 0.97 from [0.3 : 2.0]
  'attr(info="bulk Fermi potential" unit = "V")
parameter real Kp = 150e-6 from [10e-6 : inf]
  'attr(info="transconductance parameter" unit = "A/V**2")
parameter real Theta = 50e-3 from [0.0 : inf]
  'attr(info="mobility reduction coefficient" unit = "1/V")
parameter real EO = 88.0e6 from [1.0e6 : inf]
  'attr(info="mobility coefficient" unit = "V/m")
parameter real Ucex = 1.7e-6 from [2.0e6 : 25.0e6]
  'attr(info="longitudinal critical field" unit = "V/m")

// Channel length and charge sharing parameters
parameter real Lambda = 0.23 from [0.1 : inf]
  'attr(info="depletion length coefficient")
parameter real Weta = 0.05 from [0.0 : inf]
  'attr(info="narrow channel effect coefficient")
parameter real Leta = 0.28 from [0.0 : inf]
  'attr(info="longitudinal critical field")

// Reverse short channel effect parameters
parameter real Q0 = 280e-6 from [0.0 : inf]
  'attr(info="reverse short channel charge density" unit = "A*s/m**2")
parameter real Lk = 0.5e-6 from [0.0 : inf]
  'attr(info="characteristic length" unit = "m")

// Intrinsic model temperature parameters
parameter real Tcv = 1.5e-3
  'attr(info="threshold voltage temperature coefficient" unit = "V/K")
parameter real Bex = -1.5
  'attr(info="mobility temperature coefficient")
parameter real Ucox = 1.7
  'attr(info="Longitudinal critical field temperature exponent")
parameter real Ibtt = 0.0
  'attr(info="Ibb temperature coefficient" unit = "1/K")

// Series resistance calculation parameters
parameter real Hdif = 0.9e-6 from [0.0 : inf]
  'attr(info="heavily doped diffusion length" unit = "m")
parameter real Rsh = 510.0 from [0.0 : inf]
  'attr(info="drain/source diffusion sheet resistance" unit = "Ohm/square")
parameter real Rsc = 0.0 from [0.0 : inf]
  #attr (info="source_contact_resistance" unit="Ohm")
parameter real Rdc = 0.0 from [0.0 : inf]
  #attr (info="drain_contact_resistance" unit="Ohm")
// Gate overlap capacitances
parameter real Cgso = 1.5e-10 from [0.0 : inf]
  #attr (info="gate_to_source_overlap_capacitance" unit="F/m")
parameter real Cgdo = 1.5e-10 from [0.0 : inf]
  #attr (info="gate_to_drain_overlap_capacitance" unit="F/m")
parameter real Cgbo = 4.0e-10 from [0.0 : inf]
  #attr (info="gate_to_bulk_overlap_capacitance" unit="F/m")
// Impact ionization related parameters
parameter real Iba = 2e8 from [0.0 : inf]
  #attr (info="first_impact Ionization_coefficient" unit="1/m")
parameter real Ibb = 3.5e8 from [1.0e8 : inf]
  #attr (info="second_impact Ionization_coefficient" unit="V/m")
parameter real Ibn = 1.0 from [0.1 : inf]
  #attr (info="saturation_voltage_factor_for_impact_Ionization")
parameter real Ibn = 1.0 from [0.0 : inf]
  #attr (info="flicker_noise_coefficient")
parameter real Ibn = 1.0 from [0.0 : inf]
  #attr (info="flicker_noise_exponent")
// Matching parameters
parameter real Avto = 0.0 from [0.0 : inf]
  #attr (info="area_related_threshold_voltage_mismatch_parameter" unit="V\text{m}")
parameter real Akp = 0.0 from [0.0 : inf]
  #attr (info="area_related_gain_mismatch_parameter" unit="m")
parameter real Agamma = 0.0 from [0.0 : inf]
  #attr (info="area_related_body_effect_mismatch_parameter" unit="\text{sqrt(V)}\text{m}")
// Diode parameters
parameter real N=1.0 from [1e-6:inf]
  #attr (info="emission_coefficient")
parameter real Is=1e-14 from [1e-20:inf]
  #attr (info="saturating_current" unit="A")
parameter real Bv=100 from [1e-6:inf]
  #attr (info="reverse_breakdown_voltage" unit="V")
parameter real Ibv=1e-3 from [1e-6:inf]
  #attr (info="current_at_reverse_breakdown_voltage" unit="A")
parameter real Vj=1.0 from [1e-6:inf]
  #attr (info="junction_potential" unit="V")
parameter real Cj0=300e-15 from [0:inf]
  #attr (info="zero-bias_junction capacitance" unit="F")
parameter real M=0.5 from [1e-6:inf]
  #attr (info="grading_coefficient")
parameter real Area=1.0 from [1e-3:inf]
  #attr (info="diode_relative_area")
parameter real Fc=0.5 from [1e-6:inf]
  #attr (info="forward-bias_depletion_capcitance_coefficient")
parameter real Tt=0.1e-9 from [1e-20:inf]
  #attr (info="transit_time" unit="s")
parameter real Xti=3.0 from [1e-6:inf]
  #attr (info="saturation_current_temperature_exponent")
// Temperature parameters
parameter real Tnom = 26.85
  #attr (info="parameter_measurement_temperature" unit = "Celsius")
// Local variables
real epsilon_s, epsilon_ox, Tnomk, T2, Tratio, Vto_T, Ucrit_T, Egnom, Eg, Phi_T;
real Weff, Leff, RDeff, RSeff, con1, con2, Vtoa, Kpa, Kpa_T, Gamma0, C_ox, xi;
real nn, deltaV_RSC, Vg, Vs, Vd, Vgs, Vgd, Vdsd2, Vc, Vf, VS, VD;
real VGprime, VP0, VSprime, VDprime, Gamma0, Gammaprime, Vp;
real n, X1, iff, X2, ir, Vc, Vdss, Vdssprime, deltaV, Vip;

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real Lc, DeltaL, Lprime, Lmin, Leq, X3, irprime, Beta0, eta;
real Qb0, Beta0prime, nq, Xf, Xr, qD, qS, qI, qB, Beta, Ispecific, Ids, Vib, Idb, Ibb, T;
real A, B, Vt, T2, Eg, T1, Eg, T2, Vj, T2, Cj0, T2, F1, F2, F3, Ispecific, T2;
real Id1, Id2, Id3, Id4, Is1, Is2, Is3, Is4, V1, V2, Ib_d, Ib_s, Qd, Qs, Qd1, Qd2, Qs1, Qs2;
real qb, qg, qgso, qgdo, qgbo, fourkt, Sthermal, gm, Sflicker, StoDswap, p_nMOS;

// analog begin
// Equation initialization
p_nMOS = 1.0; // nMOS
A=7.02e-4;
B=1108.0;
epsilon_s = 1.0359e-10; // Eqn 4
epsilonnox = 3.453143e-11; // Eqn 5
Tnomk = Tnom+273.15; // Eqn 6
T2=$temperature;
Tratio = T2/Tnomk;
Vto_T = Vto_T−Tcv∗(T2−Tnomk);
Egnom = 1.16−0.000702∗Tnomk∗Tnomk/(Tnomk+1108);
Eg = 1.16−0.000702∗T2∗T2/(T2+1108);
Phi_T = Phi∗Tratio−3.0∗$vt∗ln(Tratio)−Egnom∗Tratio+Eg;
Ibb_T = Ibb∗(1.0+Ibbt∗(T2−Tnomk));
Weff = W + Dw; // Eqn 25
Leff = L + Dl; // Eqn 26
RDeff = ( (Hdif∗Rsh)/Weff )/Np + Rdc;
RSeff = ( (Hdif∗Rsh)/Weff )/Np + Rsc;
con1 = sqrt(Np∗Weff∗Ns∗Leff);
Vt_T2='P_PK∗T2/'P_Q;
Eg_T1=Eq−A∗Tnomk∗Tnomk/(B+Tnomk);
Eg_T2=Eq−A∗T2/T2/(B+T2);
Vj_T2=(T2/Tnomk)∗(1−M)∗(1−pow((1−Fc)∗(1−M)));
F2=pow((1−Fc), (1+M));
F3=1−Fc∗(1+M);
Is_T2=Istab∗(T2/Tnomk)∗(Xti/N)∗limexp((-Eg_T1/Vj_T2)∗(1−T2/Tnomk));
con2 = (Cox∗Ns∗Np∗Weff∗Leff);
fourkt = 4.0∗'P_PK∗T2;
if (LEVEL == 2) begin
Ucrit_T = Ucrit∗pow(Tratio, Uce);
Vtoa = Vto+Avto/con1; // Eqn 27
Kpa = Kpa∗pow(Tratio, Bex); // Eqn 18
Gammaa = Gamma+Agamma/con1; // Eqn 29
C_epsilon = 4.0∗pow(22−3, 2); // Eqn 30
xi = 0.028∗(10.0∗(Leff/Lk)−1.0); // Eqn 31
nnn = 1.0+0.5∗(xi+ sqrt(pow(xi, 2) + C_epsilon));
deltaV_RSCE = (2.0∗Q0/Cox)∗(1.0/pow(nnn, 2)); // Eqn 32
end
// // Model branch and node voltages //
Vg = p_nMOS∗V(Gate, Bulk);
Vs = p_nMOS∗V(Source, Bulk);
Vd = p_nMOS∗V(Drain, Bulk);
VG=Vg; // Eqn 22
if ( (Vd−Vs) >= 0.0) begin
StoDswap = 1.0;
VS=Vs; // Eqn 23
$V_D = V_d; \quad // \text{Eqn 24}$

```plaintext
else
    begin
        $\text{StoDswap} = -1.0$;
        $V_D = V_s$;
        $V_S = V_d$;
    end

if (LEVEL == 2)
    $V_{G\prime} = V_g - V_{T0} + \Phi T + \Gamma a \times \sqrt{\Phi T} + \Gamma 0$;
else
    $V_{G\prime} = V_g - V_{T0} + \Phi T + \Gamma 0$;

// if (LEVEL == 2)
begin
    if (VGprime > 0)
        $V_{P0} = V_{G\prime} - \Phi T - \Gamma a \times \sqrt{V_{G\prime} + 0.75 \times \Gamma a}$;
    else
        $V_{P0} = -\Phi T$;
end
else
    begin
        if (VGprime > 0)
            $V_{P0} = V_{G\prime} - \Phi T - \Gamma a \times \sqrt{V_{G\prime} + 0.5 \times \Gamma a}$;
        else
            $V_{P0} = -\Phi T$;
end
```

$n = 1.0 + \Gamma a / (2.0 \times \sqrt{V_{P0} + \Phi T + 4.0 \times \psi T})$;

```
// if (LEVEL == 2)
begin
    $V_c = U_{crit,T} * N_s * L_{eff}$; \quad // \text{Eqn 45}
    $V_{dss} = V_c * \sqrt{0.25 + (0.25 \times V_{dss}/V_c) * \sqrt{i f f}} - 0.5$; \quad // \text{Eqn 46};
    \begin{align*}
        V_{dssprime} &= V_c * \sqrt{(0.25 + (0.25 \times V_{dss}/V_c) * \sqrt{i f f} - 0.75 \times \ln(i f f)) - 0.5} \\
                       &\phantom{=} - \psi T \times \ln((V_c/(2.0 \times \psi T)) - 0.6); \quad // \text{Eqn 47}
    \end{align*}
    \text{if} (\Lambda a * \sqrt{i f f} > V_{dss}/\psi T) \rightarrow
    \begin{align*}
        \text{deltaV} &= 4.0 \times \psi T \times \sqrt{\Lambda a * \sqrt{i f f} - (V_{dss}/\psi T)} \\
                       &\phantom{=} + (1.0/64.0); \quad // \text{Eqn 48}
    \end{align*}
else
    $\text{deltaV} = 1.0/64.0$;
end
```

$V_{dso2} = (V_D - V_S)/2$; \quad // \text{Eqn 49}
$V_{ip} = \sqrt{(pow(V_{dss}, 2) + pow(\text{deltaV}, 2)) - \sqrt{pow((V_{dso2} - V_{dss}), 2) + pow(\text{deltaV}, 2)}}$; \quad // \text{Eqn 50}

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\[ Lc = s q r t \left( \frac{\epsilon_{s i}}{C_{ox}} \cdot X_j \right) ; \]  // Eqn 51

\[ \text{Delta}_L = \Lambda \cdot Lc \cdot \ln \left( 1.0 + \left( \frac{V_{dso2} - V_{ip}}{Lc \cdot U_{crit}} \right) \right) ; \]  // Eqn 52

\[ X_3 = \left( V_{dso2} - V_{ip} \right) - \left( \frac{V_{dso2} - V_{dssprime}}{Lc \cdot U_{crit}} \right) ; \]  // Eqn 53

\[ L_{\text{min}} = N_s \cdot L_{\text{eff}} / 10.0 ; \]  // Eqn 54

\[ L_{\text{eq}} = 0.5 \cdot \left( L_{\prime} + s q r t \left( \left( L_{\prime} \right)^2 + \left( L_{\text{min}} \right)^2 \right) \right) ; \]  // Eqn 55

\[ X_3 = \left( V_{p} - V_{dso2} - V_{s} - s q r t \left( \left( V_{dssprime} \right)^2 + \left( \delta V \right)^2 \right) + s q r t \left( \left( V_{dso2} - V_{dssprime} \right)^2 + \left( \delta V \right)^2 \right) \right) / \sqrt{v_t} ; \]  // Eqn 56

\[ \text{Beta} = K_{p_a} \cdot T \cdot \left( N_p \cdot \text{Weff} / L_{\text{eq}} \right) ; \]  // Eqn 58

\[ n_q = 1.0 + \frac{\gamma_a}{2 \cdot \sqrt{v_t + \phi_T + 1 \cdot e^{-6}}} ; \]  // Eqn 69
\[ q_{gbo} = C_{gbo} \times L e f t * N_p * V_G; \]

// Drain and source diodes
if (StoDswap > 0.0)
begin
V1 = p_n_MOS \times V(Bulk, Drain_int);
V2 = p_n_MOS \times V(Bulk, Source_int);
end
else
begin
V2 = p_n_MOS \times V(Bulk, Drain_int);
V1 = p_n_MOS \times V(Bulk, Source_int);
end

Id1 = (V1 > -5.0 \times N \times N_p \times V_t) ? Area \times \Delta s \times (\limexp \left( \frac{V1}{N \times V_2 + V_t} \right) - 1.0) : 0;
Qd1 = (V1 > +5.0 \times N \times N_p \times V_t) ? (Tt + Id1 + Area \times (\limexp \left( \frac{V1}{N \times V_2 + V_t} \right) - 1.0)) : 0;

Id2 = (V1 < -5.0 \times N \times N_p \times V_t) ? Area \times \Delta s \times (\limexp \left( \frac{V1}{N \times V_2 + V_t} \right) - 1.0) : 0;
Qd2 = (V1 < +5.0 \times N \times N_p \times V_t) ? (Tt + Id2 + Area \times (\limexp \left( \frac{V1}{N \times V_2 + V_t} \right) - 1.0)) : 0;

If (StoDswap > 0.0)
begin
if (RDeff > 0.0)
begin
I(Drain, Drain_int) -= V(Drain, Drain_int)/RDeff;
else
I(Drain, Drain_int) -= V(Drain, Drain_int)/1e-7;
if (RSeff > 0.0)
begin
I(Source, Source_int) -= V(Source, Source_int)/RSeff;
else
I(Source, Source_int) -= V(Source, Source_int)/1e-7;
I(Drain_int, Source_int) += p_n_MOS \times \Delta s;
end
else
I(Drain_int, Bulk) += p_n_MOS \times \Delta s;
I(Gate, Drain_int) += p_n_MOS \times 0.5 \times \Delta t \times (\Delta q);
I(Gate, Source_int) += p_n_MOS \times 0.5 \times \Delta t \times (\Delta q);
I(Drain_int, Bulk) += p_n_MOS \times 0.5 \times \Delta t \times (\Delta q);
I(Gate, Source_int) += p_n_MOS \times \Delta t \times (\Delta q);
I(Drain_int, Bulk) += p_n_MOS \times \Delta t \times (\Delta q);
I(Gate, Source_int) += p_n_MOS \times \Delta t \times (\Delta q);
I(Drain_int, Bulk) += p_n_MOS \times (\Delta q);
I(Bulk, Drain_int) += p_n_MOS \times (\Delta q);
I(Bulk, Source_int) += p_n_MOS \times (\Delta q);
I(Bulk, Source_int) += p_n_MOS \times (\Delta q);
I(Drain_int, Source_int) += \text{white\_noise}(\text{Thermal}, \text{thermal});
I(Gate, Source_int) += \text{flicker\_noise}(\text{Flicker}, \text{Af}, \text{flicker});
I(Drain, Drain_int) += \text{white\_noise}(\text{fourkt}/RDeff, \text{thermal});
I(Source, Source_int) += \text{white\_noise}(\text{fourkt}/RSeff, \text{thermal});
end
else
begin
if (RSeff > 0.0)
  \( I(\text{Drain}, \text{Drain}_{\text{int}}) \leq V(\text{Drain}, \text{Drain}_{\text{int}})/R_{\text{Seff}}; \)
else
  \( I(\text{Drain}, \text{Drain}_{\text{int}}) \leq V(\text{Drain}, \text{Drain}_{\text{int}})/1e^{-7}; \)
if (RDeff > 0.0)
  \( I(\text{Source}, \text{Source}_{\text{int}}) \leq V(\text{Source}, \text{Source}_{\text{int}})/R_{\text{Deff}}; \)
else
  \( I(\text{Source}, \text{Source}_{\text{int}}) \leq V(\text{Source}, \text{Source}_{\text{int}})/1e^{-7}; \)
if (LEVEL == 2)
  \( I(\text{Source}_{\text{int}}, \text{Bulk}) \leq p_{\text{n-MOS}} \ast I_{\text{ds}}; \)
else
  \( I(\text{Gate}, \text{Source}_{\text{int}}) \leq p_{\text{n-MOS}} \ast 0.5 \ast \text{ddt}(qg); \)
  \( I(\text{Gate}, \text{Drain}_{\text{int}}) \leq p_{\text{n-MOS}} \ast 0.5 \ast \text{ddt}(qb); \)
  \( I(\text{Gate}, \text{Drain}_{\text{int}}) \leq p_{\text{n-MOS}} \ast \text{ddt}(qgs); \)
  \( I(\text{Gate}, \text{Source}_{\text{int}}) \leq p_{\text{n-MOS}} \ast \text{ddt}(qgs); \)
  \( I(\text{Gate}, \text{Source}_{\text{int}}) \leq p_{\text{n-MOS}} \ast \text{ddt}(qgb); \)
  \( I(\text{Gate}, \text{Source}_{\text{int}}) \leq p_{\text{n-MOS}} \ast \text{ddt}(qgbo); \)
  \( I(\text{Bulk}, \text{Source}_{\text{int}}) \leq p_{\text{n-MOS}} \ast \text{Id}_{\text{b}}; \)
  \( I(\text{Bulk}, \text{Source}_{\text{int}}) \leq p_{\text{n-MOS}} \ast \text{ddt} \ast (Q_{\text{d}}); \)
  \( I(\text{Bulk}, \text{Source}_{\text{int}}) \leq p_{\text{n-MOS}} \ast \text{ddt} \ast (Q_{\text{d}}); \)
  \( I(\text{Bulk}, \text{Source}_{\text{int}}) \leq p_{\text{n-MOS}} \ast \text{ddt} \ast (Q_{\text{b}}); \)
  \( I(\text{Source}_{\text{int}}, \text{Drain}_{\text{int}}) \leq \text{white-noise(Sthermal, "thermal");} \)
  \( I(\text{Source}_{\text{int}}, \text{Drain}_{\text{int}}) \leq \text{flicker-noise(Sflicker, A_f, "flicker");} \)
  \( I(\text{Source}_{\text{int}}, \text{Source}) \leq \text{white-noise(fourkt/RDeff, "thermal");} \)
  \( I(\text{Drain}_{\text{int}}, \text{Drain}) \leq \text{white-noise(fourkt/RSeff, "thermal");} \)
end
endendmodule

6.7.2 pMOS: EKV equation numbers are given on the right-hand side of code lines

```plaintext
// Qucs EPFL-EKV 2.6 pMOS model:
// The structure and theoretical background to the EKV 2.6
// Verilog—a model is presented in the Qucs EPL-EKV 2.6 report.
// Typical parameters are for 0.5um CMOS (C) EPFL-LEG 1999.
// Geometry range: Short channel: W >= 0.8um, L >= 0.5um
// Long channel: W >= 2um, L >= 2um
// Voltage range: |Vgb| < 3.3V, |Vdb| < 3.3V, |Vsb| < 2V
// This is free software; you can redistribute it and/or modify
// it under the terms of the GNU General Public License as published
// by the Free Software Foundation; either version 2, or (at your option)
// any later version.
// Copyright (C), Mike Brinson, mbrin72043@yahoo.co.uk, May 2008.

#include "disciplines.vams"
#include "constants.vams"

module EKV26pMOS (Drain, Gate, Source, Bulk);
inout Drain, Gate, Source, Bulk;
electrical Drain, Gate, Source, Bulk;
// Internal nodes
electrical Drain_{int}, Source_{int};
#define attr(txt) (*txt*)
```

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// Device dimension parameters
parameter real LEVEL = 1 from [1 : 2];
  'attr(info="long\_channel\_length\_parameter" unit="m");
parameter real L = 0.5e-6 from [0.0 : inf]
  'attr(info="length\_parameter" unit="m");
parameter real W = 10e-6 from [0.0 : inf]
  'attr(info="Width\_parameter" unit="m");
parameter real Np = 1.0 from [1.0 : inf]
  'attr(info="parallel\_multiple\_device\_number");
parameter real Ns = 1.0 from [1.0 : inf]
  'attr(info="series\_multiple\_device\_number");

// Process parameters
parameter real Cox = 3.45e-3 from [0 : inf]
  'attr(info="gate\_oxide\_capacitance\_per\_unit\_area" unit="F/m\^{2}");
parameter real Xj = 0.15e-6 from [0.01e-6 : 1.0e-6]
  'attr(info="metal\_junction\_depth" unit="m");
parameter real Dw = -0.03e-6 from [-inf : 0.0]
  'attr(info="channel\_width\_correction" unit="m");
parameter real Di = -0.05e-6 from [-inf : 0.0]
  'attr(info="channel\_length\_correction" unit="m");

// Basic intrinsic model parameters
parameter real Vto = -0.55 from [-inf : -1e-6]
  'attr(info="long\_channel\_threshold\_voltage" unit="V");
parameter real Gamma = 0.69 from [0.0 : 2.0]
  'attr(info="body\_effect\_parameter" unit="V^{1/2}");
parameter real Phi = 0.87 from [0.3 : 2.0]
  'attr(info="Fermi\_potential" unit="V");
parameter real Kp = 35e-6 from [1e-6 : inf]
  'attr(info="transconductance\_parameter" unit="A/V^{2}");
parameter real Theta = 50e-3 from [0.0 : inf]
  'attr(info="mobility\_reduction\_coefficient" unit="1/V");
parameter real EO = 51.0e6 from [1.0e6 : inf]
  'attr(info="mobility\_coefficient" unit="V/m");
parameter real Ucrit = 18.0e6 from [2.0e6 : 25.0e6]
  'attr(info="longitudinal\_critical\_field" unit="V/m");

// Channel length and charge sharing parameters
parameter real Lambda = 1.1 from [0.1 : inf]
  'attr(info="depletion\_length\_coefficient");
parameter real Weta = 0.0 from [0.0 : inf]
  'attr(info="narrow\_channel\_effect\_coefficient");
parameter real Leta = 0.45 from [0.0 : inf]
  'attr(info="longitudinal\_critical\_field");

// Reverse short channel effect parameters
parameter real Q0 = 200e-6 from [0.0 : inf]
  'attr(info="reverse\_short\_channel\_charge\_density" unit="A*s/m^{2}");
parameter real Lk = 0.6e-6 from [0.0 : inf]
  'attr(info="characteristic\_length" unit="m");

// Intrinsic model temperature parameters
parameter real Tcv = -1.4e-3
  'attr(info="threshold\_voltage\_temperature\_coefficient" unit="V/K");
parameter real Bex = -1.4
  'attr(info="mobility\_temperature\_coefficient");
parameter real Uex = 2.0
  'attr(info="Longitudinal\_critical\_field\_temperature\_exponent");
parameter real Ibbt = 0.0
  'attr(info="Ibb\_temperature\_coefficient" unit="1/K");

// Series resistance calculation parameters
parameter real Hdif = 0.9e-6 from [0.0 : inf]
  'attr(info="heavily\_doped\_diffusion\_length" unit="m");
parameter real Rsh = 990.0 from [0.0 : inf]
  'attr(info="drain/source\_diffusion\_sheet\_resistance" unit="Ohm/square");
parameter real Rsc = 0.0 from [0.0 : inf]

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parameter real Rdc = 0.0 from [0.0 : inf]
parameter real Cgsd = 1.5e-10 from [0.0 : inf]
parameter real Cgsd = 4.0e-10 from [0.0 : inf]
parameter real Cgso = 1.5e-10 from [0.0 : inf]
parameter real Cgdo = 1.5e-10 from [0.0 : inf]
parameter real Cgbo = 4.0e-10 from [0.0 : inf]
parameter real Iba = 0.0 from [0.0 : inf]
parameter real Ibb = 3.0e8 from [1.0e8 : inf]
parameter real Ibn = 1.0 from [0.1 : inf]
parameter real Kf = 1.0e-28 from [0.0 : inf]
parameter real Af = 1.0 from [0.0 : inf]
parameter real Avto = 0.0 from [0.0 : inf]
parameter real Akp = 0.0 from [0.0 : inf]
parameter real Agamma = 0.0 from [0.0 : inf]
parameter real N=1.0 from [1e-6:inf]
parameter real Is=1e-14 from [1e-20:inf]
parameter real Bv=100 from [1e-6:inf]
parameter real Vj=1.0 from [1e-6:inf]
parameter real Cj0=300e-15 from [0:inf]
parameter real M=0.5 from [1e-6:inf]
parameter real Area=1.0 from [1e-3:inf]
parameter real Fc=0.5 from [1e-6:inf]
parameter real Tt=0.1e-9 from [1e-20:inf]
parameter real Xti=3.0 from [1e-6:inf]
parameter real Thom = 26.85
parameter real epsilonsi, epsilonox, Tnomk, T2, Tratio, Vto,T, Ucrit_T, Egnom, Eg, Phi_T;
real Weff, Leff, RDeff, RSeff, con1, con2, Vtoa, Vp, Kpa, Kps,T, GammaA, Cepsilon; x1;
real mnn, deltaVRCSE, Vg, Vs, Vd, Vgs, Vgd; Vds2, Vg, VS, VD;
real Vprime, VP0, Vprime, VDprime, GammaA, Gammaprime, Vp;
real n, X1, iff, X2, ir, Vc, Vdssprime, deltaV, Vip;
real Lc, DeltaL, Lprime, Lmin, Leq, X3, irprime, Beta0, eta;
// Equation initialization
\[ p_{n\_MOS} = -1.0; \] // pMOS
A=7.02e-4;  // Eqn 1
B=1108.0;  // Eqn 2
\[ \epsilon_{si} = 1.0359e^{-10}; \] // Eqn 3
\[ \epsilon_{ox} = 3.453143e^{-11}; \] // Eqn 4
Tnomk = Tnom+273.15;  // Eqn 5
T2=$temperature;  // Eqn 6
Tratio = T2/Tnomk;  // Eqn 7
\[ V_{to\_T} = V_{to}+T_{cv}\times(T2-T_{nomk}); \] // Eqn 8
\[ \Phi_{T} = \Phi_{T}\times Tratio - 3.0\times Vt\times \ln(Tratio) - E_{nom}\times Tratio + E_{g}; \] // Eqn 9
\[ I_{bb\_T} = I_{bb}\times(1.0+I_{bbt}\times(T2-T_{nomk})); \] // Eqn 10
\[ W_{eff} = W + Dw; \] // Eqn 11
\[ L_{eff} = L + Dl; \] // Eqn 12
\[ R_{Deff} = ((H_{dif}\times R_{sh})/W_{eff})/N_{p} + R_{dc}; \] // Eqn 13
\[ R_{Seff} = ((H_{dif}\times R_{sh})/W_{eff})/N_{p} + R_{sc}; \] // Eqn 14
\[ con1 = sqrt(N_{p}\times W_{eff}\times N_{s}\times L_{eff}); \] // Eqn 15
\[ V_{t2}=P_{K}\times T2/P_{Q}; \] // Eqn 16
\[ V_{to\_T} = V_{to}+T_{cv}\times(T2-T_{nomk}); \] // Eqn 17
\[ E_{g\_T1} = E_{g}\times A\times T_{nomk}/(B+T_{nomk}); \] // Eqn 18
\[ E_{g\_T2} = E_{g}\times A\times T_{T2}/(B+T_{T2}); \] // Eqn 19
\[ V_{j2}=V_{j}(1-M)\times((1-F_{c})\times(1-M)); \] // Eqn 20
\[ F_{1} = (V_{j}\times(1-M))\times(1-pow((1-F_{c})\times(1-M))); \] // Eqn 21
\[ F_{2} = pow((1-F_{c})\times(1-M)); \] // Eqn 22
\[ F_{3} = 1-F_{c}\times(1-M); \] // Eqn 23
\[ Is_{T2} = Is_{T2}\times pow((T2-T_{nomk})\times(X_{ti}/N)); \] // Eqn 24
\[ fourkt = 4.0\times P_{K}\times T2; \] // Eqn 25

if (LEVEL == 2)
begin
\[ U_{crit\_T} = U_{crit}\times pow(Tratio, U_{ce}); \] // Eqn 26
\[ V_{toa} = V_{toa}/con1; \] // Eqn 27
\[ K_{pa} = K_{pa}\times pow( Tratio, B_{ex}); \] // Eqn 28
\[ Gamma = Gamma+Agamma/con1; \] // Eqn 29
\[ C_{e_{psilon}} = 4.0\times pow(2e^{-3}, 2); \] // Eqn 30
\[ xi = 0.028\times(10.0\times(Leff/Lk)-1.0); \] // Eqn 31
\[ ann = 1.0+0.5\times(xi+ sqrt(pow(xi, 2)+C_{e_{psilon}})); \] // Eqn 32
\[ \delta_{RSCE} = (2.0\times Q_{0}/C_{ox})\times(1.0/pow(ann, 2)); \] // Eqn 33
end

// Model branch and node voltages
//
\[ V_{g} = p_{n\_MOS}\times V\text{(Gate, Bulk)}; \] // Eqn 34
\[ V_{s} = p_{n\_MOS}\times V\text{(Source, Bulk)}; \] // Eqn 35
\[ V_{d} = p_{n\_MOS}\times V\text{(Drain, Bulk)}; \] // Eqn 36
\[ V_{G} = V_{g}; \] // Eqn 37
if ( (V_{d}-V_{s}) >= 0.0)
begin
StoDswap = 1.0;  // Eqn 38
\[ VS=Vs; \] // Eqn 39
\[VD=Vd; \] // Eqn 40
end
end

else
    begin
        StoDswap = -1.0;
        VD=Vs;
        VS=Vd;
    end

if (LEVEL == 2)
    VGprime=VG-Vto_T-delta_V_RSC+Phi_T+Gamma*sqrt (Phi_T);  // Eqn 33 nMOS equation
else
    VGprime=Vg-Vto_T+Phi_T+Gamma*sqrt (Phi_T);

if (LEVEL == 2)
    begin
        if (VGprime > 0)
            VP0=VGprime-Phi_T+Gammaa*sqrt (Gammaa/2.0) + (Gammaa/2.0) - (Gammaa/2.0);
            // Eqn 34
        else
            VP0 = -Phi_T;

        VSprime = 0.5*(VS+Phi_T+sqrt (pow ((VS+Phi_T),2) + pow (4.0*$vt,2))) ; // Eqn 35
        VDprime=0.5*(VD+Phi_T+sqrt (pow ((VD+Phi_T),2) + pow (4.0*$vt,2))) ; // Eqn 35
    end
else
    begin
        if (VGprime > 0)
            VP = VGprime-Phi_T+Gamma*sqrt (Gamma/2.0) + (Gamma/2.0) - (Gamma/2.0);
            // Eqn 34
        else
            VP = -Phi_T;

        n = 1.0 +Gammaa/(2.0*sqrt (VP+Phi_T+4.0*$vt)) ; // Eqn 39
    end

end

//
// X1 = (VP-VS)/$vt;
// X2 = (VP-VD)/$vt;
// X3 = ln (1.0+limexp (X1/2.0)) + ln (1.0+limexp (X2/2.0)) ; // Eqn 44
// X4 = (VP-VD)/$vt;
if (LEVEL == 2)
    begin
        Vc = Ucrit_T*Ns*Leff; // Eqn 45
        Vdssprime = Vc*(sqrt (0.25 + ($vt/(Vc))*sqrt (iff)) - 0.5); // Eqn 46;
        Vdssprime = Vc*(sqrt (0.25 + ($vt/(Vc))*sqrt (iff)) - 0.75*ln (iff)) - 0.5)
            +$vt*(ln (Vc/(2.0*$vt)) - 0.6); // Eqn 47
        deltaV = 4.0*$vt+sqrt (Lambda*sqrt (iff)) - (Vdss/$vt) + (1.0/64.0) ; // Eqn 48
    end
else
    deltaV = 1.0/64.0;
    Vdss2 = (VD-VS)/2.0;  // Eqn 49
    Vip = sqrt ( pow (Vdss2, 2) + pow (deltaV,2)) - sqrt ( pow ((Vdss2 - Vdss), 2)
            + pow (deltaV, 2));  // Eqn 50
    Lc = sqrt ( (epsilonsi/Cox)*Xj); // Eqn 51
    DeltaL = Lambda*Lc*ln (1.0+((Vdss2-Vip)/(Lc*Ucrit_T)) ); // Eqn 52
    Lprime = Ns*Leff - DeltaL + ( (Vdss2+Vip)/Ucrit_T); // Eqn 53
    Lmin = Ns*Leff/10.0; // Eqn 54
\[ \text{Leq} = 0.5 \cdot (\text{Lprime} + \sqrt{\text{pow}(\text{Lprime}, 2) + \text{pow}(\text{Lmin}, 2)}) \quad \text{// Eqn 55} \]

\[ \text{X3} = (Vp-Vdso2-\text{VS}-\sqrt{\text{pow}(\text{Vdssprime}, 2) + \text{pow}(\delta V, 2)}) \]
\[ + \sqrt{\text{pow}(\text{Vdso2}-\text{Vdssprime}, 2) + \text{pow}(\delta V, 2)}) / \delta \text{v}; \]

\[ \text{irprime} = \ln(1.0+\limexp(X3/2.0) \times \ln(1.0+\limexp(X3/2.0))) \quad \text{// Eqn 56} \]

\[ \text{Beta0} = \text{Kps}_T \times (N_p \times \text{Weff} / \text{Leq}); \quad \text{// Eqn 58} \]

\[ \text{eta} = 0.3333333; \quad \text{// Eqn 59 - pMOS} \]

\[ \text{Qb0} = \text{Gamma} \times \sqrt{\phi_{\text{I}}}; \quad \text{// Eqn 60;} \]

\[ \text{Beta0prime} = \text{Beta0} \times (1.0 + (\text{Cox} / (\text{EO} \times \epsilon_{\text{psilonsi}})) \times \text{Qb0}); \quad \text{// Eqn 61} \]

\[ \text{nq} = 1.0 + \text{Gamma} \times (\text{Vp} / \text{Phi}_T + 1 \times 10^{-6}); \quad \text{// Eqn 69} \]

\[ \text{end} \]

\[ \text{end} \]

\[ \text{else} \]

\[ \text{nq} = 1.0 + \text{Gamma} / (2.0 \times \sqrt{\text{Vp} + \phi_{\text{I}}}); \quad \text{// Eqn 69} \]

\[ \text{//} \]

\[ \text{Xf} = \sqrt{0.25 + \text{iff}}; \quad \text{// Eqn 70} \]

\[ \text{Xr} = \sqrt{0.25 + \text{ir}}; \quad \text{// Eqn 71} \]

\[ \text{qD} = -\text{nq} \times ((4.0/15.0) + (3.0 \times \text{pow}(Xr, 3) + 6.0 \times \text{pow}(Xr, 2) \times \text{Xf} + 4.0 \times \text{Xr} \times \text{pow}(Xf, 2) \quad + 2.0 \times \text{pow}(\text{Xf}, 3) / \text{pow}(\text{Xf} + \text{Xr}, 2)) \quad - 0.5) \quad \text{// Eqn 72} \]

\[ \text{qS} = -\text{nq} \times ((4.0/15.0) + (3.0 \times \text{pow}(Xf, 3) + 6.0 \times \text{pow}(Xf, 2) \times \text{Xr} + 4.0 \times \text{Xr} \times \text{pow}(Xr, 2) \quad + 2.0 \times \text{pow}(Xr, 3) / \text{pow}(\text{Xf} + \text{Xr}, 2) \quad - 0.5) \quad \text{// Eqn 73} \]

\[ \text{qL} = -\text{nq} \times ((4.0/3.0) + (\text{pow}(\text{Xf}, 2) + (\text{Xf} \times \text{Xr}) + \text{pow}(\text{Xr}, 2) / (\text{Xf} + \text{Xr}) - 1.0); \quad \text{// Eqn 74} \]

\[ \text{if} \quad (\text{LEVEL} == 2) \]

\[ \quad \text{if} \quad (\text{VGprime} > 0) \]

\[ \quad \text{qB} = (-\text{Gamma} \times \sqrt{\text{Vp} + \phi_{\text{I}} + 1 \times 10^{-6}}) \times (1.0 / \delta \text{v}) - (\text{nq} - 1.0) / \text{nq} \times qI; \quad \text{// Eqn 75} \]

\[ \text{else} \]

\[ \quad \text{qB} = -\text{VGprime} / \delta \text{v}; \quad \text{//} \]

\[ \text{else} \]

\[ \quad \text{if} \quad (\text{VGprime} > 0) \]

\[ \quad \text{qB} = (-\text{Gamma} \times \sqrt{\text{Vp} + \phi_{\text{I}} + 1 \times 10^{-6}}) \times (1.0 / \delta \text{v}) - (\text{nq} - 1.0) / \text{nq} \times qI; \quad \text{// Eqn 75} \]

\[ \text{else} \]

\[ \quad \text{qB} = -\text{VGprime} / \delta \text{v}; \quad \text{//} \]

\[ \text{if} \quad (\text{LEVEL} == 2) \]

\[ \quad \text{Beta} = \text{Beta0prime} / (1.0 + (\text{Cox} / (\text{EO} \times \epsilon_{\text{psilonsi}})) \times \text{svt} \times \text{abs}(\text{qB} + \text{eta} \times \text{qI}); \quad \text{// Eqn 62} \]

\[ \text{else} \]

\[ \quad \text{Beta} = \text{Kp} \times (\text{Weff} / \text{Leff}) / (1 + \text{Theta} \times \text{Vp}); \quad \text{// Eqn 63} \]

\[ \text{Ispecific} = 2.0 \times \text{n} \times \text{Beta} \times \text{pow}(\delta \text{v}, 2); \quad \text{// Eqn 65} \]

\[ \text{if} \quad (\text{LEVEL} == 2) \]

\[ \quad \text{begin} \]

\[ \quad \text{Ids} = \text{Ispecific} \times (\text{iff} - \text{irprime}); \quad \text{// Eqn 66} \]

\[ \quad \text{Vib} = \text{VD-\text{VS}-\text{Ibn} \times 2.0 \times \text{Vds}; \quad \text{// Eqn 67} \]

\[ \quad \text{if} \quad (\text{Vib} > 0.0) \]

\[ \quad \text{ldb} = \text{Ids} \times (\text{Ibn} / \text{IbnT}) \times \text{Vib} \times \text{exp} \times (-\text{IbnT} \times \text{Leff}) / \text{Vib}; \quad \text{// Eqn 68} \]

\[ \quad \text{else} \]

\[ \quad \text{ldb} = 0.0; \quad \text{//} \]

\[ \quad \text{end} \]

\[ \text{else} \]

\[ \quad \text{Ids} = \text{Ispecific} \times (\text{iff} - \text{ir}); \quad \text{// Eqn 66} \]

\[ \text{//} \]

\[ \text{Stermal} = \text{fourK} \times \text{Beta} \times \text{abs}(\text{qI}); \]

\[ \text{gm} = \text{Beta} \times \delta \text{v} \times (\text{pow}(4.0 \times \text{iff} / \text{Ispecific} + 1.0) - \sqrt{\text{pow}(4.0 \times \text{ir} / \text{Ispecific} + 1.0)}); \quad \text{// Eqn 71} \]

\[ \text{Sflicker} = (\text{Kf} \times \text{gm} / \text{Np} \times \text{Weff} \times \text{Ns} \times \text{Leff} \times \text{Cox}); \quad \text{// Eqn 72} \]

\[ \text{qb} = \text{con2} \times \delta \text{v} \times \text{qbB}; \quad \text{// Eqn 73} \]

\[ \text{qgso} = \text{Cgso} \times \text{Weff} \times \text{Np} \times (\text{VG-\text{VS}}); \quad \text{// Eqn 74} \]

\[ \text{qgdo} = \text{Cgdo} \times \text{Weff} \times \text{Np} \times (\text{VG-\text{VD}}); \quad \text{// Eqn 75} \]

\[ \text{qgbo} = \text{Cgbo} \times \text{Leff} \times \text{Np} \times \text{VG}; \quad \text{// Eqn 76} \]

\[ \text{if} \quad (\text{StoDswap} > 0.0) \]

\[ \text{begin} \]
\begin{verbatim}
V1=p_nMOS*V(Bulk, Drain_int);
V2=p_nMOS*V(Bulk, Source_int);
end
else
    begin
        V2=p_nMOS*V(Bulk, Drain_int);
        V1=p_nMOS*V(Bulk, Source_int);
        end
    Id1=(V1>-5.0*N*$vt) ? Area*Is_T2*(limexp((V1/(N*Vt_T2)) -1.0) : 0;
    Qd1=(V1<=5.0*N*$vt) ? Area*Is_T2 * (1 - pow((1 - V1/Vt_T2), (1 - M)));:
    Id2=(V1<-5.0*N*$vt) ? Area*Is_T2 : 0;
    Qd2=(V1<=-5.0*N*$vt) ? Area*Is_T2 * (1 - pow((1 - V1/Vt_T2), (1 - M)));
    s = Is1+Is2+Is3+Is4;
    T2 = Id1+Id2+Id3+Id4;
    Qd = Qd1+Qd2;
// Current contributions
if (StoSswap > 0.0)
    begin
        if (RDeff > 0.0)
            I(Drain, Drain_int) <- V(Drain, Drain_int)/RDeff;
        else
            I(Source, Source_int) <- V(Source, Source_int)/RSeff;
        else
            I(Drain_int, Source_int) <- V(Source, Source_int)/1e-7;
        end
    if (LEVEL == 2)
        I(Drain_int, Bulk) <- p_nMOS*Ids;
        I(Gate, Drain_int) <- p_nMOS*0.5*ddt(qg);
        I(Gate, Source_int) <- p_nMOS*0.5*ddt(qb);
        I(Drain_int, Bulk) <- p_nMOS*0.5*ddt(qq);
        I(Source_int, Bulk) <- p_nMOS*0.5*ddt(qd);
        I(Gate, Source_int) <- p_nMOS*ddt(qsco);
        I(Gate, Drain_int) <- p_nMOS*ddt(qgdo);
        I(Bulk, Drain_int) <- p_nMOS*ddt(qgbo);
        I(Bulk, Drain_int) <- p_nMOS*1b_d;
        I(Bulk, Drain_int) <- p_nMOS*ddt(Qd);
        I(Bulk, Source_int) <- p_nMOS*1b_s;
        I(Bulk, Source_int) <- p_nMOS*ddt(Qs);
        I(Drain_int, Source_int) <- white_noise(Sthermal,"thermal");
        I(Drain_int, Source_int) <- flicker_noise(Sflicker, AF, "flicker");
        I(Drain, Drain_int) <- white_noise(fourkt/RDeff, "thermal");
        I(Source, Source_int) <- white_noise(fourkt/RSeff, "thermal");
        end
    else
        begin
            if (RSeff > 0.0)
                I(Drain, Drain_int) <- V(Drain, Drain_int)/RSeff;
            else

    end
end
\end{verbatim}
I(Drain, Drain_int) <= V(Drain, Drain_int)/1e-7;
if (RDeff > 0.0)
    I(Source, Source_int) <= V(Source, Source_int)/RDeff;
else
    I(Source, Source_int) <= V(Source, Source_int)/1e-7;
( Source_int, Drain_int ) <= p_n_MOS*Ids;
if (LEVEL == 2)
    I(Source_int, Bulk) <= p_n_MOS*Idb;
I(Gate, Source_int) <= p_n_MOS*0.5*ddt(qg);
I(Gate, Drain_int) <= p_n_MOS*0.5*ddt(qg);
I(Source_int, Bulk) <= p_n_MOS*0.5*ddt(qb);
I(Drain_int, Bulk) <= p_n_MOS*0.5*ddt(qb);
I(Gate, Drain_int) <= p_n_MOS*ddt(qgso);
I(Gate, Source_int) <= p_n_MOS*ddt(qgdo);
I(Gate, Bulk) <= p_n_MOS*ddt(qgbo);
I(Bulk, Source_int) <= p_n_MOS*Idb;
I(Bulk, Source_int) <= p_n_MOS*ddt(Qd);
I(Bulk, Drain_int) <= p_n_MOS*Is;
I(Bulk, Drain_int) <= p_n_MOS*ddt(Qs);
I(Source_int, Drain_int) <= white_noise(Sthermal,"thermal");
I(Source_int, Drain_int) <= flicker_noise(Sflicker, Af, "flicker");
I(Source_int, Source) <= white_noise(fourkt/RDeff, "thermal");
I(Drain_int, Drain) <= white_noise(fourkt/RSeff, "thermal");
end
end
endmodule
6.8 Update number one: September 2008

The first version of the Qucs EPFL-EKV v2.6 model provided Qucs users with reasonably complete long and short channel models for nMOS and pMOS devices. In no respect were these models optimized for minimum simulation run time or were they flexible enough to allow users to select the style of charge partitioning employed by the EKV model. Recent work on the Qucs implementation of the EKV v2.6 MOSFET model and the Qucs ADMS/XML interface has resulted in a significant reduction in simulation run time overhead, particularly in transient and small signal analysis. The addition of a SPICE BSIM style partition parameter Xpart to the Qucs version of the EKV v2.6 model now allows users to set the style of charge partitioning employed by the EKV model. These notes explain the function of the first EKV v2.6 update and introduce a series of test simulations that demonstrate the effects these changes have on the operation of the Qucs port of the EKV V2.6 model.

6.8.1 Model initialisation

Readers who have looked through the EKV v2.6 Verilog-A code listed in the previous sections of these notes will probably have been struck by the quantity of calculations involved each time the code is evaluated during simulation. In the case of transient analysis it is calculated at least once per time step, often resulting in many thousands of passes through the code. The more MOS devices included in a circuit the greater the time overhead becomes. Obviously, a sensible approach would be to minimize the amount of calculation by only evaluating once those parts of the EKV model equations which result in constant values during simulation. The Verilog-A hardware description language provides a model initialisation feature which selects those parts of a device model code which are to be evaluated prior to the start of a simulation. The resulting calculated variables are then available for use by other sections of the Verilog-A model code during simulation. In transient and small signal analysis this is particularly important as it significantly reduces simulation calculation time. Verilog-A employs the “at” (@(initial_step) or @(initial_model) ) language construction coupled with a begin ... end block to signify the Verilog-A code that is to be evaluated only at model initialisation. Although this technique does greatly improve model simulation speed it does imply significantly more work for the model developer in that the Verilog-A device code has to be split into initialisation and dynamic simulation sections. Readers interested in the detail of how this split can be achieved should compare the latest EKV v2.6 Verilog-A CVS code given at the Qucs Web site with that presented in previous sections of these notes.
6.8.2 Charge partitioning

The MOSFT is a four terminal device with a dynamic performance that requires accurate calculation of the charge at each terminal. Previous notes indicated that the intrinsic channel charge equals the sum of the drain and source charges. However, the exact proportion of intrinsic channel charge that belongs to the drain or to the source is often not known. The assignment of the proportion of the channel charge to the drain and source charges is called charge partitioning. The first release of the Qucs EKV v2.6 model used the 50/50 partitioning scheme where 50% of the channel charge is arbitrarily assigned to both drain and source. It’s interesting to note that this partitioning scheme has no physical basis but depends entirely on convenience. A second partitioning scheme, called the 40/60 partitioning, does however, have a strong physical basis\(^9\). Yet a third charge partitioning is often employed for digital circuit simulation; this is known as the 0/100 partition. The second release of the Qucs EPFL-EKV v2.6 model includes an extra parameter called Xpart which allows users to set the partitioning scheme for dynamic simulation calculations. Xpart default is set at 0.4 which corresponds to the 40/60 partitioning scheme. Figure 6.10 illustrates a test circuit for determining the S-Parameters of an nMOS device connected as a capacitance. Both the device capacitance and associated series resistance can be extracted from S[1,1]. Qucs equation block Eqn1 gives the equations for extracting these properties. Other equations in Eqn1 show how the extracted capacitance can be represented as a ratio of the basic parallel capacitance given by

\[
C_{\text{parallel, plate}} = W \cdot L \cdot Cox. \quad (6.30)
\]

6.8.3 Modelling EKV v2.6 charge partitioning using Qucs EDD

Complex simulation results like those shown in Fig 6.10 suggest the question “How do we check the accuracy of the model being simulated?” One possible approach is to develop a second model of the same device based on the same physical principles and equations but using a different approach like the Qucs EDD/subcircuit modelling route shown in Fig. 6.11. It is an EDD/subcircuit model of a long channel EKV v2.6 nMOS device which includes charge partitioning. Figure 6.12 illustrated the same test circuit as Fig. 6.10 and the extracted capacitance and resistance values for the EDD model of the long channel nMOS device. A number of features observed from Fig. 6.10 and Fig. 6.11 are worth commenting on; firstly that good agreement is recorded between the two sets of results, secondly that

Figure 6.10: Test circuit for simulating EKV v2.6 charge partitioning effects: Xpart = 0.4 or QD/QS = 40/60
the Verilog-A model includes both overlap capacitance and drain and gate source resistances. Hence the slight difference in the capacitance ratio and the recorded values of Rin above one Ohm for the Verilog-A model.
Figure 6.11: Qucs EDD model for a EKV v2.6 long channel nMOS device with charge partitioning
Figure 6.12: Test circuit for simulating EKV v2.6 EDD model charge partitioning effects: $X_{part} = 0.4$ or $QD/QS = 40/60$
6.9 End note

The first update of the Qucs EKV v2.6 model provides users with a more optimised model, with improved simulation performance and a more complete charge partitioning scheme. Even with these changes the model is still not complete. The nMOS and pMOS Verilog-A code needs to be unified and a number of optional parameters need to be added to the Qucs implementation of the EKV v2.6 model. The next update of the model is scheduled for the near future, following correction of bug reports sent in by Qucs users. Once again my thanks to Stefan Jahn for all his help and support during the first EKV v2.6 update development phase.
7 Compact Verilog-A pn junction photodiode model

7.1 Introduction

Optoelectronic devices are not included in Qucs version 0.0.14 or earlier releases of the software. With the growing importance of these devices, and indeed the fact that they are present in an increasing number of electronic systems, this is a significant omission. This report presents the structure and physical details of a Qucs implementation of a pn junction photodiode model. The photodiode model is the first in a planned series of Verilog-a compact device models for optoelectronic components. The report also introduces the concept of a light bus and shows how light paths can be added to Qucs simulation schematics. A number of example schematics are also included in the report to demonstrate the performance of the new Verilog-A pn junction photodiode model. The background to the work outlined in this report was first published in the International Journal of Numerical Modelling: Electronic Networks, Devices and Fields in September 2008\(^1\).

7.2 pn junction photodiode effects modelled

The Qucs pn junction photodiode model includes the following features:

- Diode photocurrent response characteristics expressed as a function of light power and wavelength.
- Diode DC I-V characteristics in the forward and reverse bias regions including avalanche breakdown in reverse bias.
- Diode bias dependent capacitance.
- Diode shunt resistance.

- Diode package series resistance.
- Device noise, including thermal, shot, flicker and quantum contributions.

### 7.3 The Qucs pn junction photodiode model

The schematic capture symbol and equivalent electrical circuit for the Qucs pn junction photodiode is shown in Fig. 7.1. In this model the DC properties and capacitance of the photodiode are represented by a semiconductor diode with a parallel shunt resistance $R_{\text{sh}}$. Device lead resistance is represented by series resistance $R_{\text{series}}$. A voltage-controlled current source models the diode photocurrent. The gain of the controlled source is set as the responsivity of the photodiode. The equivalent circuit shown in Fig. 7.1(c) presents the complete photodiode model with thermal, shot and flicker noise sources included. One interesting, and unusual, feature of the Qucs photodiode noise model is the inclusion of quantum shot noise, modelled by noise current source $I_{\text{lightn}}$. Photocurrent $I_{\text{light}}$ is given by

$$I_{\text{light}} = \text{Light} \cdot \text{Responsivity} \quad (7.1)$$

where $\text{Light}$ is the optical signal in W and $\text{Responsivity}$ is the spectral responsivity in A/W. Responsivity can also be written in terms of the photodiode quantum efficiency given by

$$\text{Responsivity} = \frac{QE \cdot q \cdot \lambda}{h \cdot c} = \frac{\text{QE}_{\text{percent}} \cdot \lambda}{1.2398 \times 10^{-5}} \quad (7.2)$$

where $QE$ is the photodiode quantum efficiency, $\lambda$ is the light wavelength in nm, $h$ is Plank’s constant, $c$ is the speed of light in a vacuum, and $QE_{\text{percent}}$ is the quantum efficiency given in percentage. In Fig. 7.1 the optical signal path is shown as a green line connected at the side of the photodiode symbol. In Qucs simulations optical signals are modelled as voltage quantities expressed as real numbers, even though they represent a power quantity, and are shown on a schematic as green connecting lines between components. This has the effect of clearly identifying optical signal paths on a schematic, when compared to the blue lines which indicate connecting wires characterised by conventional current and voltage signals. Similarly, signal sources which input light to a circuit are coloured green, see later example simulations.
7.3.1 Photodiode parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
<th>Default</th>
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<tbody>
<tr>
<td>N</td>
<td>N</td>
<td>photodiode emission coefficient</td>
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<td>Is</td>
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<td>Bv</td>
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<td>V</td>
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<td>Ibv</td>
<td>current at reverse breakdown voltage</td>
<td>A</td>
<td>1e-3</td>
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<td>M</td>
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<td>Temp</td>
<td>device temperature</td>
<td>°C</td>
<td>26.85</td>
</tr>
</tbody>
</table>

* Parameter LEVEL is used to select how the photodiode Responsivity is determined: with LEVEL = 1 the model uses the listed value of parameter Responsivity or calculates its value if QEpercent is not equal to zero; with LEVEL = 2 Responsivity is always calculated using QEpercent.

7.3.2 pn junction photodiode model equations

- Basic semiconductor DC characteristics
  \[ I_d = I_1 + I_2 + I_3 + I_4 \]  

  Where
  1. \[ I_1 = \text{Area} \cdot I_s(T2) \cdot \left[ \log_{10} \left( \frac{V_d}{N \cdot V_t(T2)} \right) - 1 \right] + V_d \cdot GMIN \quad \forall (V_d > -5 \cdot N \cdot V_t) \]
  2. \[ I_2 = -\text{Area} \cdot I_s(T2) + V_d \cdot GMIN \quad \forall (-Bv < V_d) \text{ and } (V_d > -5 \cdot N \cdot V_t) \]
  3. \[ I_3 = -I_{Bv} \quad \forall (V_d = -Bv) \]
1. \( C_{\text{diff}} = \frac{dQ_{\text{diff}}}{dVd} = Tt \cdot \frac{Id}{dVd} \)

2. \( C_{\text{dep}} = \frac{dQ_{\text{dep}}}{dVd} = \text{Area} \cdot Cj0 \cdot \left(1 - \frac{Vd}{Vj}\right)^{-M} \)

where \( Qd = Q_{\text{dep}} + Q_{\text{diff}} \), and

\[
Qd = Tt \cdot Id + \frac{\text{Area} \cdot Cj0 \cdot Vj}{1 - M} \left\{ 1 - \left(1 - \frac{Vd}{Vj}\right)^{-M} \right\} \forall (Vd < Fc \cdot Vj)
\]

\[
Qd = Tt \cdot Id + \text{Area} \cdot Cj0 \cdot \left\{ F1 + \frac{1}{F2} \left( F3 \cdot (Vd - Fc \cdot Vj) + \left[ \frac{M}{2 \cdot Vj} \right] \cdot [Vd^2 - (Fc \cdot Vj)^2] \right) \right\} \forall (Vd > Fc \cdot Vj)
\]

Where

\[
F1 = \frac{Vj}{1 - M} \cdot \left[ 1 - (1 - Fc)^{-M} \right]
\]

\[
F2 = [1 - Fc]^{1+M}
\]

\[
F3 = 1 - Fc \cdot (1 + M)
\]

and \( \text{GMIN} = 1 \cdot 10^{-12} \text{S} \).

- Diode area factors
  1. \( I_{\text{s,area}} = I_s \cdot \text{Area} \)
  2. \( C_{\text{j0,area}} = Cj0 \cdot \text{Area} \)
  3. \( R_{\text{series,area}} = \frac{R_{\text{series}}}{\text{Area}} \)

- Diode temperature factors
  1. \( I_{\text{s}}(T2) = I_s \cdot \left\{ \frac{T2}{T1} \right\}^{Xti} \cdot \frac{N}{\text{limexp}} \left\{ \frac{-Eg(T1)}{Vt(T2)} \cdot \left[ 1 - \frac{T2}{T1} \right] \right\} \)
  2. \( Vj(T2) = \frac{T2}{T1} \cdot Vj - 2 \cdot Vt(T2) \cdot \ln \left( \frac{T2}{T1} \right)^{1.5} - \left\{ \frac{T2}{T1} \cdot Eg(T1) - Eg(T2) \right\} \)
  3. \( Cj0(T2) = Cj0 \cdot \left\{ 1 + M \cdot \left[ 400e - 6 \cdot (T2 - T1) - \frac{Vj(T2)}{Vj} \right] \right\} \)

Where

\[
T1 = T_{\text{nom}} + 273.15, \quad T2 = T_{\text{temp}} + 273.15
\]

\[
Eg(T) = EG(0) - \frac{7.02e - 4 \cdot T^2}{1108 + T}
\]
\[ V_{t1} = \frac{K \cdot T_1}{q}, \quad V(t_2) = \frac{K \cdot T_2}{q} \] and \( K \) and \( q \) have their usual meaning.

- Diode photocurrent

\[ I_{light} = Light \cdot Responsivity \] (7.5)

Where \( Responsivity = \frac{Q \cdot q \cdot \lambda}{h \cdot c} = \frac{QE \cdot \lambda}{1.2398 \cdot 55} \)

- Photodiode noise

\[ I_{pd\_noise}^2 = I_{Rshn}^2 \cdot \Delta f + I_{dsn}^2 \cdot \Delta f + I_{dfn}^2 \cdot \Delta f + I_{lightn}^2 \cdot \Delta f \] (7.6)

Where \( I_{Rshn}^2 = \frac{4 \cdot K \cdot T}{R_{sh}}, \quad I_{dsn}^2 = 2 \cdot q \cdot I_d, \quad I_{dfn}^2 = \frac{K \cdot I_f \cdot D \cdot f}{f^{f_f}}, \quad I_{light}^2 = 2 \cdot q \cdot I_{light} \), and \( \Delta f \) is the noise frequency bandwidth in Hz.

### 7.3.3 Verilog-A model code

```verilog
// Qucs compact photodiode model
// The structure and theoretical background to the photodiode
// Verilog-a model are presented in the Qucs photodiode report.
// This is free software; you can redistribute it and/or modify
// it under the terms of the GNU General Public License as published by
// the Free Software Foundation; either version 2, or (at your option)
// any later version.
// Copyright (C), Mike Brinson, mbrin72043@yahoo.co.uk, October 2008.

#include "disciplines.vams"
#include "constants.vams"

module photodiode (Anode, Cathode, Light);
inout Anode, Cathode, Light;
electrical Anode, Cathode, Light;
electrical ni;

'define attr(txt) (*txt*)

parameter real N=1.35 from [1e-6:inf]
  'attr (info="photodiode\_emission\_coefficient");
parameter real Rseries=1e-3 from [1e-6:inf]
  'attr (info="series\_lead\_resistance" unit = "Ohm");
parameter real Is=0.34e-12 from [1e-20:inf]
  'attr (info="diode\_dark\_current" unit="A");
parameter real Bv=60 from [1e-6:inf]
  'attr (info="reverse\_breakdown\_voltage" unit="V");
parameter real Ibv=1e-3 from [1e-6:inf]
```
\[
\begin{align*}
\text{parameter } & \text{ real } V_j = 0.7 \text{ from } [1e-6:inf] \\
\text{parameter } & \text{ real } C_{j0} = 60e-12 \text{ from } [0:inf] \\
\text{parameter } & \text{ real } M = 0.5 \text{ from } [1e-6:inf] \\
\text{parameter } & \text{ real } \text{Area} = 1.0 \text{ from } [1.0:inf] \\
\text{parameter } & \text{ real } \text{Vt} = 26.85 \text{ from } [-273:inf] \\
\text{parameter } & \text{ real } \text{Fc} = 0.5 \text{ from } [1e-6:inf] \\
\text{parameter } & \text{ real } \text{Tt} = 10e-9 \text{ from } [1e-20:inf] \\
\text{parameter } & \text{ real } \text{Xti} = 3.0 \text{ from } [1e-6:inf] \\
\text{parameter } & \text{ real } \text{Eg} = 1.16 \text{ from } [1e-6:inf] \\
\text{parameter } & \text{ real } \text{Responsivity} = 0.5 \text{ from } [1e-6:inf] \\
\text{parameter } & \text{ real } \text{Rsh} = 5e8 \text{ from } [1e-6:inf] \\
\text{parameter } & \text{ real } \text{Kf} = 1e-12 \text{ from } [0:inf] \\
\text{parameter } & \text{ real } \text{Af} = 1.0 \text{ from } [0:inf] \\
\text{parameter } & \text{ real } \text{Ffe} = 1.0 \text{ from } [0:inf] \\
\text{model } & \text{branches} \\
\text{branch} \ (\text{Anode, n1}) \ b6; \\
\text{branch} \ (\text{n1, Cathode}) \ b1; \\
\text{initial} \ & \text{step} \\
\text{begin} \\
\text{end}
\end{align*}
\]
GMIN=1e^-12;
Cj0,T2=Cj0*(1+M*(400e^-6*(T2-T1)-(Vj_T2-Vj)));
Is_T2=Is*pow((T2/T1),(Xti/N))*limexp((-Eg*T1)/$vt*(1-T2/T1));
Res1=(QEpercent != 0) ? QEpercent*Lambda/1.2398e5:Responsivity;
Res2=QEpercent*Lambda/1.2938e5;
Res=(LEVEL==1) ? Res1 : Res2;
con1=-5.0*N*Vt;
con2=Area*Is_T2;
con3=Area*Cj0_T2;
con4=Fc*Vj;
con5=Fc*Vj_T2;
con6=Bv/Vt_T2;
end
// Current contributions
V1=V(b1);
I1=(V1 > con1) ? con2*(limexp(V1/(N*Vt_T2))-1.0)+GMIN*V1 : 0;
I2=(V1 <= con1) ? -con2+GMIN*V1 : 0;
I3=(V1 < -Bv)?-Ibv : 0;
I4=(V1<con4) ? Tt*I1 + con3*(Vj_T2/(1-M))*(1-pow((1-V1/Vj_T2),(1-M))):0;
Q1=(V1<con4) ? Tt*I1 + con3*(F1/(1/F2))*(F3*(V1-con5)+(M/(2.0*Vj_T2))*(V1-V1-con5*con5)) : 0;
I5=V(Light)*Res;
Id=I1+I2+I3+I4;
I(b1) <+ -15;
I(b1) <+ V(b1)/Rsh;
I(b6)<+V(b6)/Rseries_Area;
I(b1)<+Id;
I(b1)<+ddt(Q1+Q2);
I(Light)<+V(Light)/1e10;
// Noise contributions
fourkt=4.0*P_K*$temperature;
TwoQ=2.0*P_Q;
I_flicker=power(Id, Af);
I(b6)<+white_noise(fourkt/Rseries_Area, "thermal");
I(b1)<+white_noise(fourkt/Rsh, "thermal");
I(b1)<+white_noise(TwoQ*Id, "shot");
I(b1)<+flicker_noise(Kf*I_flicker, Ffe, "flicker");
I(b1)<+white_noise(TwoQ*I5, "shot");
//
end
endmodule
7.4 Example photodiode circuits

Figure 7.2: Basic photodiode test circuit for simulating device output current as a function of light input level and applied DC bias
Figure 7.3: Photodiode test circuit for extracting device capacitance and resistance as a function of applied DC bias
Figure 7.4: Pulsed light power comparator circuit using two photodiodes and a logarithmic amplifier
Figure 7.5: Photodiode noise test circuit and simulated noise characteristics
7.5 End Note

Optoelectronic devices are an important group of electronic components and as such deserve more attention than has been given to them in the past by the Qucs development team. This situation should improve over the coming year. The pn junction photodiode model is the first in a planned series of optoelectronic models, including models for transimpedance amplifiers, optical actuators and optical media. Given time it should be possible to significantly improve Qucs optoelectronic capabilities. The photodiode model reported here is an interesting model in that it is one of the first Verilog-A models to fully utilize the recent changes to the ADMS/Qucs interface which allow proper initialisation of model parameters. A new procedure for combining Verilog-A generated models also introduces for the first time the initial stages towards a fully modularized approach to linking complex models with the main body of the Qucs code. Once again my thanks to Stefan Jahn for all his encouragement and help during the period I worked on the photodiode model.
8 SPICE to Qucs conversion: Test File 1

8.1 Introduction

8.1.1 Title
DC and independent voltage pulse generator test.

8.1.2 Test file name

8.1.3 SPICE specification

Format:
\texttt{VX N+ N- [[DC] DC/TRAN VALUE] [AC [ACMAG [ACPHASE]]]}

Notes:
1. Characters [ and ] enclose optional items
2. Character / denotes OR
3. Independent voltage source names begin with the letter V
4. X denotes name of source
5. N+ and N- are the positive and negative nodes respectively
6. Voltage sources need not be grounded

Specification of SPICE statement being tested:
\texttt{VX N+ N- [[DC] VALUE] [PULSE(V1 V2 [ TD [ TR [ TF [ PW [PER]]]]])] Notes:}

1. PULSE generates a periodic pulse, where
2. V1 is the initial value; default: must be specified
3. V2 is the pulsed value; default: must be specified

4. TD is the delay time; default value = TSTEP

5. TR is the rise time; default value = TSTEP

6. TF is the fall time; default value = TSTEP

7. PW is the pulse width; default value = TSTOP

8. PER is the period; default value = TSTOP

### 8.2 Test code and schematic

SPICE code: File `S2Q_test1.cir`

```plaintext
* SPICE to Qucs syntax test file 1.
* DC and independent voltage pulse sources, plus resistors.
* .subckt S2Q_test1 p01 p02 p03 p04 p05 p06 p07 p08 p09 p10 p11
  v1 p01 0 1v
  r1 p01 0 10k
  *
  v2 p02 0 dc 1v
  r2 p02 0 10k
  *
  v3 p03 0 pulse(0 5)
  r3 p03 0 10k
  *
  v4 p04 0 pulse(0 5 20n)
  r4 p04 0 10k
  *
  v5 p05 0 pulse(0 5 20n 10n)
  r5 p05 0 10k
  *
  v6 p06 0 pulse(0 5 20n 10n 10n)
  r6 p06 0 10k
  *
  v7 p07 0 pulse(0 5 20n 10n 10n 50n)
  r7 p07 0 10k
  *
  v8 p08 0 pulse(0 5 20n 10n 10n 50n 100n)
  r8 p08 0 10k
```
Figure 8.1: SPICE to Qucs conversion: Test1

* v9 p09 0 pulse(0 5 20n 1n 1n 20n 40n)
  r9 p09 0 10k
* v10 p10 0 pulse(0 5 20n 0.1n 0.1n 0.5n 5n 50n)
  r10 p10 0 10k
* v11 p11 0 dc 5v pulse(0 5 20n 0.5n 0.5n 10n 20n)
  r11 p11 0 10k
.ends
.end

8.3 History of simulation results

8.3.1 March 8 2007, Simulation tests by Mike Brinson

1. Test 1: Vp1.Vt; Pass correct result.

2. Test 2: Vp2.Vt; Pass correct result.

3. Test 3: Vp3.Vt; Fail TR and TF should default to TSTEP [TSTEP=1nS in test]

4. Test 4: Vp4.Vt; Fail TR and TF should default to TSTEP [TSTEP=1nS in test]

10. Test 10 : Vp10.Vt; Fail - waveform should repeat after 70ns.
11. Test 11 : Vp11.Vt; Fail

   1. waveform should repeat after 40ns,
   2. Vdc:V11 _cnet8 _ref U="0" incorrect,
      should be Vdc:V11 _cnet8 _ref U="5"

8.3.2 March 10 2007, Simulation tests by Mike Brinson

Code modified * check_spice.cpp: Handling periodic pulse sources correctly. Also default Tr/Tf values for these sources to a given .TRAN step value: Stefan Jahn.

Restriction on SPICE code: $TD + TR + PW + TF < PER$, otherwise a negative TL time for the repetitive pulse occurs and simulation fails.

SPICE test file S2Q_test1.cir modified: Mike Brinson

Figure 8.2: Qucs netlist [Edited to fit on page width]
Figure 8.3: SPICE to Qucs conversion: Test1 simulation waveforms
SPICE to Qucs syntax test file 1.
DC and independent voltage pulse sources, plus resistors.

```
.subckt S2Q_test1 p01 p02 p03 p04 p05 p06 p07 p08 p09 p10 p11
  v1 p01 0 1v
  r1 p01 0 10k
  *
  v2 p02 0 dc 1v
  r2 p02 0 10k
  *
  v3 p03 0 pulse(0 5)
  r3 p03 0 10k
  *
  v4 p04 0 pulse(0 5 20n)
  r4 p04 0 10k
  *
  v5 p05 0 pulse(0 5 20n 10n)
  r5 p05 0 10k
  *
  v6 p06 0 pulse(0 5 20n 10n 10n)
  r6 p06 0 10k
  *
  v7 p07 0 pulse(0 5 20n 10n 10n 50n)
  r7 p07 0 10k
  *
  v8 p08 0 pulse(0 5 20n 10n 10n 50n 100n)
  r8 p08 0 10k
  *
  v9 p09 0 pulse(0 5 10n 1n 1n 20n 40n)
  r9 p09 0 10k
  *
  v10 p10 0 pulse(0 5 20n 0.1n 0.1n 5n 50n)
  r10 p10 0 10k
  *
  v11 p11 0 dc 5v pulse(-3 5 20n 0.5n 0.5n 10n 40n)
  r11 p11 0 10k
.ends
.end
```

Figure 8.4: Modified SPICE test1 netlist


11. Test 11 : Vp11.Vt; Pass
Figure 8.5: SPICE to Qucs conversion: Modified test1 simulation waveforms
Figure 8.6: Qucs netlist for modified test1 SPICE netlist [Edited to fit on page width]
8.4 References


9 SPICE to Qucs conversion: Test File 2

9.1 Introduction

9.1.1 Title
DC and independent voltage sin generator test.

9.1.2 SPICE specification

Format:
VX N+ N- [[DC] DC/TRAN VALUE] [AC [ACMAG [ACPHASE] ] ]

Notes:
1. Characters [ and ] enclose optional items
2. Character / denotes OR
3. Independent voltage source names begin with the letter V
4. X denotes name of source
5. N+ and N- are the positive and negative nodes respectively
6. Voltage sources need not be grounded

Specification of SPICE statement being tested:

VX N+ N- [[DC] VALUE] [SIN(VO VA [ FREQ [ TD [ KD ] ] ] ) ]

Notes:
1. SIN generates a periodic sinusoidal signal, where
2. VO is the DC offset; default: must be specified
3. VA is the signal amplitude; default: must be specified
4. FREQ is the signal frequency; default: value = 1/TSTOP
5. TD is initial delay before sinusoidal signal starts; default: value = 0 seconds
6. KD is the damping coefficient; default: value = 0. The damping factor has dimension 1/time.

9.2 Test code and schematic

SPICE code: File S2Q_test2.cir

* SPICE to Qucs syntax test file 2
* DC and independent voltage sin sources, plus resistors.
* .subckt S2Q_test2 p01 p02 p03 p04 p05 p06 p07 p08 p09 p10 p11
v1 p01 0 1v
r1 p01 0 10k
*v2 p02 0 dc 1v
r2 p02 0 10k
* v3 p03 0 sin(0 5)
r3 p03 0 10k
* v4 p04 0 sin( 0 5 1k)
r4 p04 0 10k
* v5 p05 0 sin(0 5 1k 0.5m)
r5 p05 0 10k
* v6 p06 0 sin(0 5 1k 0.5m 100)
r6 p06 0 10k
* v7 p07 0 sin(0 5 1k 0.5m 1000)
r7 p07 0 10k
* v8 p08 0 dc 5v sin(0 5 1k 0.5m 1000)
r8 p08 0 10k
* v9 p09 0 sin(-5 5 1k 0.5m 1000)
r9 p09 0 10k
9.3 History of simulation results

9.3.1 March 11 2007, Simulation tests by Mike Brinson

1. Test 1 : Vp1.Vt; Pass correct result.

2. Test 2 : Vp2.Vt; Pass correct result.
3. Test 3 : Vp3.Vt; **Fail** ERROR: line 17: checker error, no such variable ‘nan’ used in a ‘Vac:V3’ property **NOTE** error occurs when v3 uncommented.

4. Test 4 : Vp4.Vt; Pass

5. Test 5 : Vp5.Vt; **Fail** TD should be 0.5m seconds - otherwise OK.

6. Test 6 : Vp6.Vt; **Fail** TD should be 0.5m seconds - otherwise OK.

7. Test 7 : Vp7.Vt; **Fail** TD should be 0.5m seconds - otherwise OK.

8. Test 8 : Vp8.Vt; **Fail** TD should be 0.5m seconds - otherwise OK

9. Test 9 : Vp9.Vt; **Fail** TD should be 0.5m seconds - otherwise OK

10. Test 10 : Vp10.Vt; **Fail** TD should be 0.5m seconds - otherwise OK

11. Test 11 : Vp11.Vt; **Fail** TD should be 0.5m seconds, plus DC level wrong.

### 9.3.2 March 12 2007, Simulation tests by Mike Brinson

Code modifications:

1. *check_spice.cpp*: Fixed DC offset of sinusoidal voltage and current sources. Also apply default frequency if a transient analysis is given. Stefan Jahn

2. *vac.cpp, iac.cpp*: Adjusted time dependency of damping factor Stefan Jahn

1. Test 1 : Vp1.Vt; Pass correct result.

2. Test 2 : Vp2.Vt; Pass correct result.

3. Test 3 : Vp3.Vt; Pass - see note 1 below.


5. Test 5 : Vp5.Vt; Pass - see note 2 below.


7. Test 7 : Vp7.Vt; Pass - see note 2 below.

8. Test 8 : Vp8.Vt; Pass - see note 2 below.

Figure 9.2: March 11: Quacs netlist showing V3 error [Edited to fit on page width]


1. The SPICE SIN generator assumes that the frequency of the generated sinusoidal signal equals 1/TSTOP if not explicitly given. Hence, in such cases a .TRAN statement must be present in the simulated SPICE netlist; if a .TRAN statement is not included a default frequency of f = 1GHz is used. Also, when setting the transient simulation parameters using a Qucs transient analysis icon turn off SPICE simulation in the Edit SPICE Properties dialog box, otherwise two transient simulations are undertaken by Qucs.

2. SPICE parameter TD is treated differently by Qucs. In SPICE TD is the time from 0 seconds before the sinusoidal signal starts, causing the sinusoid to be non-linear. In Qucs TD is implemented as a phase shift of a linear sinusoidal signal. In the test example TD is 0.5m seconds which at f = 1kHz gives a phase shift of 180° and is clearly visible in the test results. An error will probably occur if TD is greater than one signal period, 1m second in the test example.

3. Changes in CVS code have resulted in correct DC levels.
Figure 9.4: March 12: SPICE to Qucs conversion: Test2 waveforms
Figure 9.5: March 12: Qucs netlist showing V3 error [Edited to fit on page width]
9.4 References


10 SPICE to Qucs conversion: Test File 3

10.1 Introduction

10.1.1 Title

SPICE 2g6 and 3f5 resistors.

10.1.2 SPICE specification

Format: SPICE 2g6\(^1\):  
\[
RX \text{ N+ N- value } [ \text{ TC=TC1 [,TC2]} ]
\]

Notes:

1. Characters [ and ] enclose optional items
2. Resistors begin with letter R.
3. X denotes name of resistor.
4. N+ and N- are the positive and negative nodes respectively.
5. Equations:

\[
TNOM = \text{Nominal temperature; default } 27^\circ \text{C.}
\]

\[
\Delta T = T - TNOM
\]

\[
R(T) = R(TNOM) + [1 + TC1 \cdot \Delta T + TC2 \cdot \Delta T^2]
\]

Format: SPICE 3f5\(^2\):

1. Standard resistors: \textbf{RX N+ N- value}
2. Semiconductor resisters:

\[
RX \text{ N+ N- [value] [mname] [L=length] [W=width] [TEMP=T]}
\]

---

\(^1\)See section 6.1, SPICE 2g6 user’s guide.

\(^2\)See sections 3.1.1 and 3.1.2, SPICE 3f6 user’s guide.
Notes:

1. Characters [ and ] enclose optional items
2. Resistors begin with letter R.
3. X denotes name of resistors.
4. N+ and N- are the positive and negative nodes respectively.
5. mname; if specified the resistance is calculated from the process information given in entry .model mname.
6. L is the length of the resistor.
7. W is the width of the resistor.
8. mname .model type R parameters:
   - TC1 : First order temperature coefficient; default 0.0.Ω/°C.
   - TC2 : Second order temperature coefficient; default 0.0. Ω/°C^2.
   - RSH : Sheet resistance; default -. Ω per square.
   - DEFW : Default width; default 1e-6m.
   - NARROW : Narrowing due to side etching; default 0.0m.
   - TNOM : Nominal temperature; default 27 °C.
9. Equations $R = RSH \cdot \frac{L - NARROW}{W - NARROW}$

$$R(T) = R(TNOM) + [1 + TC1 \cdot \Delta T + TC2 \cdot \Delta T^2]$$

Where $\Delta T = T - T_0$: T is the circuit temperature and $T_0$ the nominal temperature.

10.2 Test code and schematic

SPICE code: File S2Q_test3_a.cir

* SPICE to Qucs syntax test file
* SPICE 2g6 resistors.
* .subckt S2Q_test3_a p01 p02 p03
  v1 1 0 DC 1v
r1 1 p01 10k
r2  p01 0 10k
*
v2 2 0 dc 1v
r3 2 p02 10k tc=0.01
r4 p02 0 10k
*
v3 3 0 Dc 1v
r5 3 p03 10k tc=0.01 0.015
r6 p03 0 10k
.ends
.end
Figure 10.1: March 13: SPICE to Qucs conversion: Test3 schematic plus output table for SPICE 2g6 test1: linear resistors

SPICE code: File S2Q_test3_b.cir

* SPICE to Qucs syntax test file
* SPICE 3f5 resistors.
* .subckt S2Q_test3_a p01 p02 p03
  v1 1 0 DC 1v
  r1 1 p01 10k
  r2 p01 0 10k
* v2 2 0 dc 1v
  r3 2 p02 RMOD1 L=10u W=1u
  r4 p02 0 10k
  .model RMOD1 R(RSH=50 DEFW=2e-6 NARROW=1e-7)
* .ends
.end
### 10.3 History of simulation results

#### 10.3.1 March 13 2007, Simulation tests by Mike Brinson

A: SPICE 2g6 tests:

**Test 1** [v2, r3, v3, and r5 commented]: Linear resistors: Vp1: PASS correct output voltage.

**Test 2** [v3, and r5 commented]: SPICE 2g6 resistor with first order temperature coefficient: **FAIL** - incorrect Qucs netlist.

Qucs netlist line 14: checker error, extraneous property ‘TC’ is invalid in ‘R:R3’

Qucs netlist:

```plaintext
# Qucs 0.0.11 /media/hda2/S2Q_test3_prj/S2Q(test3_a).sch

.Def:S2Q_test3_a _net0 _net1 _net2
Sub:X1 _net0 _net1 _net2 gnd Type="S2Q_test3_a_cir"
.Def:End

.Def:S2Q_test3_a_cir _netP01 _netP02 _netP03 _ref
 .Def:S2Q_TEST3_A _ref _netP01 _netP02 _netP03
  Vdc:V1 _net1 _ref U="1V"
  R:R1 _net1 _netP01 R="10k"
  R:R2 _netP01 _ref R="10k"
  Vdc:V2 _net2 _ref U="1V"
  R:R3 _net2 _netP02 R="10k" TC="0.01"
  R:R4 _netP02 _ref R="10k"
  R:R6 _netP03 _ref R="10k"
 .Def:End
 Sub:X1 _ref _netP01 _netP02 _netP03 Type="S2Q_TEST3_A"
 .Def:End

.Sub:SUB1 vp1 vp2 vp3 Type="S2Q_test3_a"
 .DC:DC1 Temp="26.85" reltol="0.001" abstol="1uA" vntol="1uV"
  saveOPs="no" MaxIter="150" saveAll="no" convHelper="none" Solver="CroutLU"
```

**Test 3** [v2, r2, and r3 commented]: **FAIL** - netlist not passed correctly.

Qucs error message: line 14: syntax error, unexpected Floats, expecting Eol.

Qucs netlist:

```plaintext
# Qucs 0.0.11 /media/hda2/S2Q_test3_prj/S2Q(test3_a).sch
```
.Def: S2Q_test3_a_net0 net1 net2
Sub: X1 net0 net1 net2 gnd Type="S2Q_test3_a_cir"
.Def: End

.Sub: S2Q_test3_a_cir netP01 netP02 netP03 ref
.Sub: End

B: SPICE 3f5 tests

Test1: SPICE file S2Q_test3_b.cir fails to convert to Qucs netlist format, giving the following error message:
line10 : syntax error, unexpected identifier, expecting Digits or Floats.
SPICE 3f5 Semiconductor resistors not implemented?

10.3.2 March 15 2007, Simulation tests by Mike Brinson

Qucs CVS code modifications:

- * scan_spice.l: Lexer modifications for the Spice 2g6 resistor syntax were necessary. Stefan Jahn
- * parse_spice.y: Allow Spice 2g6 syntax for resistors, also fixed netlist grammar for Spice 3f5 models. Stefan Jahn
- * check_spice.cpp: Handle R semiconductor model correctly as well as the Spice 2g6 syntax for the temperature coefficients. Stefan Jahn

SPICE code: File S2Q_test3_a.cir

- Vp01.V: PASS; correct dc output.
- Vp02.V: PASS; correct dc output for TEMP=TNOM.
- Vp03.V: PASS; correct dc output for TEMP=TNOM.

NOTES:

- The Vp02 and Vp03 test results are only correct for TEMP=TNOM.
• SPICE 2g6 simulates circuit performance at temperature set by the value of TNOM; 27 °C by default.

• Circuits can be simulated at other temperatures by using a .TEMP control statement; which has the format

  .TEMP T1 [ T2 [ T3 ..... ] ]

Unfortunately the Qucsconv program does not recognise this statement so there appears to be no way of changing the temperature of SPICE 2g6 resistors that have TC1 and TC2 temperature coefficients in their netlist entries.

• Adding SPICE 2g6 statement .TEMP 50 to file S2Q_test3_a.cir gives the following error:

  spice notice, no .END directive found, continuing line 18: syntax error, unexpected Identifier, expecting $end

Qucs netlist:

```
# Qucs 0.0.11 /media/hda2/S2Q_test3_prj/S2Q(test3_a).sch

.Def:S2Q_test3_a _net0 _net1 _net2
Sub:X1 _net0 _net1 _net2 gnd Type="S2Q_test3_a_cir"
.Def:End

.Def:S2Q_test3_a_cir _netP01 _netP02 _netP03 _ref
  .Def:S2Q_TEST3_A _ref _netP01 _netP02 _netP03
  Vdc:V1 _net1 _ref U="1V"
  R:R1 _net1 _netP01 R="10k"
  R:R2 _netP01 _ref R="10k"
  Vdc:V2 _net2 _ref U="1V"
  R:R3 _net2 _netP02 R="10k" Tc1="0.01"
  R:R4 _netP02 _ref R="10k"
  Vdc:V3 _net3 _ref U="1V"
  R:R5 _net3 _netP03 R="10k" Tc1="0.01" Tc2="0.015"
  R:R6 _netP03 _ref R="10k"
  .Def:End
  Sub:X1 _ref _netP01 _netP02 _netP03 Type="S2Q_TEST3_A"
  .Def:End

.DC:DC1 Temp="50" reltol="0.001" abstol="1.pA" vntol="1.uV"
  saveOPs="no" MaxIter="150" saveAll="no" convHelper="none"
  Solver="CroutLU"
```
Figure 10.2: March 15: SPICE to Qucs conversion: SPICE 2g6 resistor schematic plus output table

Sub: SUB1 vp1 vp2 vp3 Type="S2Q_test3_a"

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
</tbody>
</table>
SPICE code: File `S2Q_test3_b.cir`

- Vp01.V: **PASS**; correct dc output.
- Vp02.V: **PASS**; correct dc output.

Qucs netlist:

```
# Qucs 0.0.11 /media/hda2/S2Q_test3_prj/S2Q(test3_b).sch

.Def:S2Q_test3_b_net0_net1
Sub:X1_net0_net1 gnd Type="S2Q_test3_b.cir"
.Def:End

.Subckt S2Q_test3_b_cir_netP01_netP02_ref
  .Def:S2Q_TEST3_A_ref_netP01_netP02
  Vdc:V1_net1_ref U="1V"
  R:R1_net1_netP01 R="10k"
  R:R2_netP01_netP02 R="10k"
  Vdc:V2_net2_ref U="1V"
  R:R3_net2_netP02 R="550"
  R:R4_netP02_ref R="10k"
  .Def:End
Sub:X1_ref_netP01_netP02 Type="S2Q_TEST3_A"
.Def:End
```

SPICE code: File `S2Q_test3_c.cir`

```
* SPICE to Qucs syntax test file
* SPICE 3f5 resistors : Temperature effects.

.subckt S2Q_test3_a p01 p02 p03 p04 p05 p06 p07 p08 p09 p10
  v1 1 0 DC 1v
  r1 1 p01 10k
  r2 p01 0 10k

  v2 2 0 dc 1v
  r3 2 p02 10k RMOD1
  r4 p02 0 10k
.model RMOD1 R(TC1=0.01 TC2=0.015)
```
Vp01.V: PASS; correct dc output.

Vp02.V: PASS; correct dc output.

Vp03.V: PASS; correct dc output.

Vp04.V: PASS; correct dc output.

Vp05.V: PASS; correct dc output.
• Vp06.V: PASS; correct dc output.
• Vp07.V: PASS; correct dc output.
• Vp08.V: PASS; correct dc output.
• Vp09.V: PASS; correct dc output.
• Vp20.V: PASS; correct dc output.

NOTES:

• In SPICE 3f5 TEMP values attached to resistors override the global value of TEMP.

• SPICE 3f5 differs from SPICE 2g6 in that it does not allow the control statement .TEMP.
Figure 10.3: March 15: SPICE to Qucs conversion: Test3 schematic plus output for SPICE 3f5 test c

Qucs netlist:

```
# Qucs 0.0.11 /media/hda2/S2Q_test3_prj/s2Q(test3_c).sch

.Def:S2Q_test3_c_net0_net1_net2_net3_net4_net5_net6_net7_net8_net9
Sub:X1_net0_net1_net2_net3_net4_net5_net6_net7_net8_net9
gnd Type="S2Q_test3_c_cir"
.Def:End

.Def:S2Q_test3_c_cir_netP01_netP02_netP03_netP04_netP05_netP06_netP07_netP08_netP09_netP10_ref
 .Def:S2Q_TEST3_A_ref_netP01_netP02_netP03_netP04_netP05_netP06_netP07_netP08_netP09_netP10
 Vdc:V1_net1_ref U="1V"
 R:R1_net1_netP01 R="10k"
 R:R2_netP01_ref R="10k"
 Vdc:V2_net2_ref U="1V"
 R:R3_net2_netP02 R="10k" Tc1="0.01" Tc2="0.015"
 R:R4_netP02_ref R="10k"
 Vdc:V3_net3_ref U="1V"
 R:R5_net3_netP03 R="10k" Temp="30" Tc1="0.01" Tc2="0.015"
 R:R6_netP03_ref R="10k"
 Vdc:V4_net4_ref U="1V"
 R:R7_net4_netP04 R="10k" Temp="40" Tc1="0.01" Tc2="0.015"
 R:R8_netP04_ref R="10k"
 Vdc:V5_net5_ref U="1V"
 R:R9_net5_netP05 R="10k" Temp="50" Tc1="0.01" Tc2="0.015"
```
10.3.3 March 18 2007, Simulation tests by Mike Brinson

More SPICE 3f5 Temperature tests.

SPICE code: File S2Q_test3_f.cir

* SPICE to Qucs syntax test file
* SPICE 3f5 resistors.
* Temperature tests.

* .subckt S2Q_test3_f p01 p02 p03 p04
v1 1 0 DC 1v
r1 1 p01 10k
r2 p01 0 10k
*
*
v2 2 0 dc 1v
r3 2 p02 10k RMOD1 TEMP=50
r4 p02 0 10k
.model RMOD1 R(TC1=0.01 TC2=0.015)
*
  v3 3 0 dc 1v
r5 3 p03 10k RMOD1
r6 p03 0 10k
.model RMOD1 R(TC1=0.01 TC2=0.015 TNOM=100)
*
  v4 4 0 dc 1v
r7 4 p04 10k RMOD1
r8 p04 0 10k
.model RMOD1 R(TC1=0.01 TC2=0.015)
*
.ends
.OPTION TNOM=40
.end

- Vp01.V: **PASS**; correct dc output.
- Vp02.V: **PASS**; correct dc output.
- Vp03.V: **FAIL**; dc output does not change with changes in .OPTION TEMP or TNOM.
- Vp04.V: **FAIL**; dc output does not change with changes in .OPTION TEMP or TNOM.

**NOTES:**
- In SPICE 3f5 TEMP values attached to resistors override the global value of circuit temperature
- Output Vp02 is correct the value of R3 being determined by TEMP=50, TC1=0.01 and TC2=0.015 during the resistance calculation.
- Using SPICE statements .OPTION TNOM=XX or .OPTION TEMP=XX appears to have no effect on resistance calculations.
- Similarly, adding TNOM=XX to a R model appears not to affect the resistance calculations.
Figure 10.4: March 18: SPICE to Qucs conversion: Test3 schematic plus output for SPICE 3f5 test f

Qucs netlist:

```plaintext
# Qucs 0.0.11 /media/hda2/S2Q_test3_prj/S2Q(test3_f).sch

.Sub: SUB1 vp01 vp02 vp03 vp04 Type="S2Q_test3_f"

.Vdc: V1 _net1 _ref U="1V"
.R: R1 _net1 _net0 _ref R="10k"
.R: R2 _net0 _ref R="10k"
.Vdc: V2 _net2 _ref U="1V"
.R: R3 _net2 _netP02 _ref R="10k" Temp="50" Tc1="0.01" Tc2="0.015"
.R: R4 _netP02 _ref R="10k"
.Vdc: V3 _net3 _ref U="1V"
.R: R5 _net3 _netP03 _ref R="10k" Tc1="0.01" Tc2="0.015"
.R: R6 _netP03 _ref R="10k"
.Vdc: V4 _net4 _ref U="1V"
.R: R7 _net4 _netP04 _ref R="10k" Tc1="0.01" Tc2="0.015"
.R: R8 _netP04 _ref R="10k"
.Sub: End

 number  vp01.V  vp02.V  vp03.V  vp04.V
 1       0.5     0.0974  0.5     0.5
```

Sub: SUB1 vp01 vp02 vp03 vp04 Type="S2Q_test3_f"
10.4 March 25 2007, Simulation tests by Mike Brinson

Code modifications:

- * scan_spice.l, parse_spice.y: Accept .TEMP syntax (Spice 2g6) in lexer and parser. Stefan Jahn.

SPICE code: File S2Q_test3_a.cir
SPICE statements .OPTION TNOM=50 and .TEMP 50 are now accepted in the SPICE to Qucs translation process. HOWEVER, at the moment (Qucs 0.0.12) global circuit temperature parameters are not implemented in the Qucs simulator and cannot be changed via these statements.

SPICE code: File S2Q_test3_f.cir
SPICE code modification due to test bug caused by RMOD1 being referenced in each test.
New code:

```
*.subckt S2Q_test3_f p01 p02 p03 p04
v1 1 0 DC 1v
r1 1 p01 10k
r2 p01 0 10k
v2 2 0 dc 1v
r3 2 p02 10k RMOD1 TEMP=50
r4 p02 0 10k
.model RMOD1 R(TC1=0.01 TC2=0.015)
v3 3 0 dc 1v
r5 3 p03 10k RMOD2
r6 p03 0 10k
.model RMOD2 R(TC1=0.01 TC2=0.015 TNOM=100)
v4 4 0 dc 1v
r7 4 p04 10k RMOD3
r8 p04 0 10k
.model RMOD3 R(TC1=0.01 TC2=0.015)
```
Figure 10.5: March 25: SPICE to Qucs conversion: Test3 schematic plus output for SPICE 3f5 test f

```
.ends
.OPTION TNAME=40
.end
```
Qucs netlist:

```
# Qucs 0.0.12 /media/hda2/S2Q_test3_prj/S2Q(test3_f).sch

.Def:S2Q_test3_f_net0 _net1 _net2 _net3
Sub:X1 _net0 _net1 _net2 _net3 gnd Type="S2Q_test3_f_cir"
.Def:End

.Def:S2Q_test3_f_cir _netP01 _netP02 _netP03 _netP04 _ref
.Def:S2Q_TEST3_F _ref _netP01 _netP02 _netP03 _netP04
  Vdc:V1 _net1 _ref U="1V"
  R:R1 _net1 _netP01 R="10k"
  R:R2 _netP01 _ref R="10k"
  Vdc:V2 _net2 _ref U="1V"
  R:R3 _net2 _netP02 R="10k" Temp="50" Tc1="0.01" Tc2="0.015"
  R:R4 _netP02 _ref R="10k"
  Vdc:V3 _net3 _ref U="1V"
  R:R5 _net3 _netP03 R="10k" Tc1="0.01" Tc2="0.015" Tnom="100"
  R:R6 _netP03 _ref R="10k"
  Vdc:V4 _net4 _ref U="1V"
  R:R7 _net4 _netP04 R="10k" Tc1="0.01" Tc2="0.015"
  R:R8 _netP04 _ref R="10k"
  .Def:End
Sub:X1 _ref _netP01 _netP02 _netP03 _netP04 Type="S2Q_TEST3_F"
.Def:End

Sub:SUB1 vp01 vp02 vp03 vp04 Type="S2Q_test3_f"
  .DC:DC1 Temp="26.8" reltol="0.001" abstol="1_pA" vntol="1_uV"
  saveOPs="no" MaxIter="150" saveAll="no" convHelper="none" Solver="CroutLU"
```

- Vp01.V: **PASS**; correct dc output.
- Vp02.V: **PASS**; correct dc output.
- Vp03.V: **PASS**; correct dc output.
- Vp04.V: **FAIL**; dc output does not change with changes in .OPTION
  TNOM = 40. The Qucs simulator does NOT implement a global
temperature parameter but allocates separate temperatures to each
component.

**NOTES:**

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• In SPICE 3f5 TEMP values attached to resistors override the global value of circuit temperature

• Output Vp02 is correct, the value of R3 being determined by TEMP=50, TC1=0.01 and TC2=0.015.

• Output Vp03 is correct, the value of R5 being determined by TNOM=100, TC1=0.01 and TC2=0.015.

• Output VP04 is 0.5 because .OPTION TNOM=40 has no effect on the temperature of resistor R8. By default the temperature of R8 is set to 26.85°C.

10.5 References


11 SPICE to Qucs conversion: Test File 4

11.1 Introduction

11.1.1 Title

SPICE 2g6 and 3f5 capacitors.

11.1.2 SPICE specification

Format: SPICE 2g6\(^1\):

1. Linear form: \( CX \ N+ \ N- \ value \ [ \ IC = \ INCOND] \)

2. Nonlinear form: \( CX \ N+ \ N- \ [POLY] \ value \ [C1 \ [ \ C2 \ ...]] \ [IC = \ INCOND] \)

Notes:

1. Characters [ and ] enclose optional items

2. Capacitors begin with letter C.

3. X denotes name of capacitor

4. N+ and N- are the positive and negative nodes respectively.

5. Equations:

   Capacitors may be nonlinear functions of voltage, where

   \[ C(V) = value + C1 \cdot V + C2 \cdot V^2 + \ldots + Cn \cdot V^n \]

Format: SPICE 3f5\(^2\):

\(^1\)See section 6.2, SPICE 2g6 user’s guide.

\(^2\)See sections 3.1.4 and 3.1.5, SPICE 3f6 user’s guide.
1. Linear capacitors: \textbf{CX N+ N- value [ IC = INCOND ]}

2. Semiconductor capacitors:
\texttt{CX N+ N- [value] [mname] [L=length] [W=width] [IC=VAL]}

Notes:

1. Characters \texttt{[} and \texttt{]} enclose optional items
2. Capacitors begin with letter C.
3. X denotes name of capacitor
4. N+ and N- are the positive and negative nodes respectively.
5. mname; if specified the capacitance is calculated from the process information given in entry .model mname.
6. L is the length of the capacitor.
7. W is the width of the capacitor.
8. mname .model type C parameters:
   - CJ : Junction bottom capacitance; default \texttt{-}\textit{F/meters^2}.
   - CJSW : Junction sidewall capacitance; default \texttt{-}\textit{F/meters^2}.
   - DEFW : Default width; default \texttt{1e-6 meters}.
   - NARROW : Narrowing due to side etching; default \texttt{0.0 meters}.
9. Equations:
\begin{align*}
CAP &= CJ \cdot (L - \text{NARROW}) \cdot (W - \text{NARROW}) + 2 \cdot CJSW \cdot (L + W - 2 \cdot \text{NARROW})
\end{align*}

\section*{11.2 Test code and schematic}

SPICE code: File \texttt{S2Q_test4_a.cir}

\begin{verbatim}
* SPICE to Qucs syntax test file
* SPICE 2g6 and 3f5 linear capacitors.
* DC and AC tests.
* .subckt S2Q_test4_a p01 p02 p03 p04 p05 p06
  v1 1 0 AC 1v
  r1 1 p01 10k
\end{verbatim}
SPICE code: File S2Q_test4_b.cir

* SPICE to Qucs syntax test file
* SPICE 2g6 and 3f5 linear capacitors.
* Pulse tests.
*.
.subckt S2Q_test4_b p01 p02 p03 p04 p05
v1 1 0 pulse(0 1 50ms 1us 1us 100ms 200ms)
r1 1 p01 10k
c1 p01 0 1u ic=0v
v2 2 0 pulse(0 1 50ms 1us 1us 100ms 200ms)
r3 2 p02 10k
c2 p02 0 1u ic = -1v
v3dc 3 0 dc 1v
v3ac 4 3 pulse(0 1 50ms 1us 1us 100ms 200ms)
r4 4 p03 10k
c4 p03 0 1u ic=0v
v4dc 5 0 dc 1v
v4ac 6 5 pulse(0 1 50ms 1us 1us 100ms 200ms)
r5 6 p04 10k
c5 p04 0 1u ic = -1v
v5 7 0 dc 1v pulse(0 1 50ms 1us 1us 100ms 200ms)
r6 7 p05 10k
c6 p05 0 1u ic = -1v.
.ends
.end

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Figure 11.1: March 22: SPICE to Qucs conversion: Test4 schematic plus dc output table for SPICE 2g6 and 3f5 linear capacitors test
11.3 History of simulation results

11.3.1 March 22 2007, Simulation tests by Mike Brinson

A: SPICE 2g6 and 3f5 linear capacitor dc tests:

- Vp01.V: **FAIL**; correct dc output = 0V.
- Vp02.V: **FAIL**; correct dc output = 0V.
- Vp03.V: **FAIL**; correct dc output = 1V.
- Vp04.V: **FAIL**; correct dc output = 1V.
- Vp05.V: **FAIL**; correct dc output = 1V.
- Vp06.V: **FAIL**; correct dc output = 1V.

NOTE: It would appear that the value of a branch AC voltage source is being added to DC sources in the same branch during the DC simulation. This is incorrect. Qucs correctly computes the DC conditions from a schematic, see Fig. 11.2. ERROR in SPICE to Qucs conversion process.
Figure 11.2: March 22: Qucs RC simulation with series AC and DC sources
Qucs netlist:

```
# Qucs 0.0.11 /media/hda2/S2Q_test4_prj/S2Q(test4_a).sch

.Def:S2Q_test4_a_cir _netP01 _netP02 _netP03 _netP04 _netP05 _netP06 _ref
.Def:S2Q_TEST4_A _ref _netP01 _netP02 _netP03 _netP04 _netP05 _netP06
Vac:V4 _net8 _cnet5 U="1V"
Vac:V3 _net7 _cnet4 U="1V"
Vac:V4AC _net6 _cnet3 U="1V"
Vac:V3AC _net4 _cnet2 U="1V"
Vac:V2 _net2 _cnet1 U="1V"
Vac:V1 _net1 _cnet0 U="1V"
Vdc:V1 _cnet0 _ref U="1"
R:R1 _net1 _netP01 R="10k"
C:C1 _netP01 _ref C="1u"
Vdc:V2 _cnet1 _ref U="1"
R:R3 _net2 _netP02 R="10k"
C:C2 _netP02 _ref C="1u" V="10V"
Vdc:V3DC _net3 _ref U="1V"
Vdc:V3AC _cnet2 _net3 U="1"
R:R4 _net4 _netP03 R="10k"
C:C3 _netP03 _ref C="1u"
Vdc:V4DC _net5 _ref U="1V"
Vdc:V4AC _cnet3 _net5 U="1"
R:R5 _net6 _netP04 R="10k"
C:C4 _netP04 _ref C="1u" V="10V"
Vdc:V3 _cnet4 _ref U="1V"
R:R6 _net7 _netP05 R="10k"
C:C5 _netP05 _ref C="1u"
Vdc:V4 _cnet5 _ref U="1V"
R:R7 _net8 _netP06 R="10k"
C:C6 _netP06 _ref C="1u" V="10V"
.Sub:End
.Sub:X1 _ref _netP01 _netP02 _netP03 _netP04 _netP05 _netP06
Type="S2Q_TEST4_A"
.Sub:End

.DC:DC1 Temp="26.85" reltol="0.001" abstol="1uA" vntol="1uV"
saveOPs="no" MaxIter="150" saveAll="no" convHelper="none" Solver="CroutLU"
Sub:X1 vp01 vp02 vp03 vp04 vp05 vp06 gnd Type="S2Q_test4_a_cir"
```
Figure 11.3: March 22: Output waveforms for ac tests

B: SPICE 2g6 and 3f5 linear capacitor ac tests:
Simulation waveforms appear to be correct, see Fig. 11.3.

C: SPICE 2g6 and 3f5 capacitor pulse tests.
SPICE code: File S2Q_test4_b.cir

Qucs netlist:
# Qucs 0.0.11 /media/hda2/S2Q_test4_prj/S2Q(test4_b).sch

`Def:S2Q_test4_b_cir _netP01 _netP02 _netP03 _netP04 _netP05 _ref
Def:S2Q_TEST4_B _ref _netP01 _netP02 _netP03 _netP04 _netP05
Vrect:V5 _net7 _cnet4 U="1" Td="50ms" Tr="1us" Tf="1us"
TH="0.100002" TI="0.049998"`
**Figure 11.4:** March 22: SPICE to Qucs conversion: Test4 schematic plus dc output table for SPICE 2g6 and 3f5 linear capacitors pulse test

```
Vrect:V4AC _net6 _cnet3 U="1" Td="50ms" Tr="1us" Tf="1us"
TH="0.100002" TI="0.049998"
Vrect:V3AC _net4 _cnet2 U="1" Td="50ms" Tr="1us" Tf="1us"
TH="0.100002" TI="0.049998"
Vrect:V2 _net2 _cnet1 U="1" Td="50ms" Tr="1us" Tf="1us"
TH="0.100002" TI="0.049998"
Vrect:V1 _net1 _cnet0 U="1" Td="50ms" Tr="1us" Tf="1us"
TH="0.100002" TI="0.049998"
Vdc:V1 _cnet0 _ref U="0"
R:R1 _net1 _netP01 R="10k"
C:C1 _netP01 _ref C="1u" V="0V"
Vdc:V2 _cnet1 _ref U="0"
R:R3 _net2 _netP02 R="10k"
C:C2 _netP02 _ref C="1u" V="-1V"
Vdc:V3DC _net3 _ref U="1V"
Vdc:V3AC _cnet2 _net3 U="0"
R:R4 _net4 _netP03 R="10k"
C:C4 _netP03 _ref C="1u" V="0V"
Vdc:V4DC _net5 _ref U="1V"
Vdc:V4AC _cnet3 _net5 U="0"
R:R5 _net6 _netP04 R="10k"
C:C5 _netP04 _ref C="1u" V="-1V"
Vdc:V5 _cnet4 _ref U="1"
R:R6 _net7 _netP05 R="10k"
```

<table>
<thead>
<tr>
<th>number</th>
<th>vp01.V</th>
<th>vp02.V</th>
<th>vp03.V</th>
<th>vp04.V</th>
<th>vp05.V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.667</td>
<td>0.667</td>
<td>1.67</td>
<td>1.67</td>
<td>1.67</td>
</tr>
</tbody>
</table>

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C: C6 _netP05 _ref C="1u" V="-1V"
  .Def: End
Sub: X1 _ref _netP01 _netP02 _netP03 _netP04 _netP05 Type="S2Q_TEST4_B"
  .Def: End

  .DC: DC1 Temp="26.85" retol="0.001" abstol="1µA" vntol="1µV"
  saveOPs="no" MaxIter="150"
  saveAll="no" convHelper="none" Solver="CroutLU"
  .TR: TR1 Type="lin" Start="0" Stop="400ms" Points="1000"
  IntegrationMethod="Gear" Order="6" InitialStep="0.01ns"
  MinStep="1e-16" MaxIter="1500" retol="0.001" abstol="100µA"
  vntol="100µV" Temp="26.85" LTEreltol="1e-3" LTEabstol="1e-6"
  LTEfactor="1" Solver="CroutLU" relaxTSR="no" initialDC="yes"
  MaxStep="0"
Sub: X1 vp01 vp02 vp03 vp04 vp05 gnd Type="S2Q_test4_b_cir"

C 1: DC simulation.
  • Vp01.V: FAIL; correct dc output = 0V.
  • Vp02.V: FAIL; correct dc output = 0V.
  • Vp03.V: FAIL; correct dc output = 1V.
  • Vp04.V: FAIL; correct dc output = 1V.
  • Vp05.V: FAIL; correct dc output = 1V.

NOTE: There appears to be an error in the dc simulation of the converted SPICE test netlist. All dc output values have roughly 0.67 volts added to their correct value. This could possibly be due to the way capacitor voltages are initialised. Qucs appears not to initialise capacitor voltages and they appear to be left floating after the SPICE to Qucs conversion process if they are not set by an IC=INCD statement? Although SPICE allows capacitor voltages to be initialised via the optional parameter IC = INCOND this is only used at the start of transient analysis. The question is does it also get used in an .op dc analysis? Here there is a problem for Qucs and possibly the best solution would be for Qucs to use the IC=INCOD value for the initial capacitor voltage, if given, otherwise set capacitor dc voltages to zero at the start of dc and transient analysis. Moreover, they must be initialised and NOT left floating at an indeterminate value.

C 2: Transient simulation:
Simulation waveforms appear to be correct, see Fig. 11.5. NOTE: The transient analysis is set to use capacitor initialisation voltages.
Figure 11.5: March 22: Pulse test waveforms for SPICE 2g6 and 3f5 linear capacitors
D: Combined DC, AC and transient source test.

SPICE code: File S2Q_test4_c.cir

* SPICE to Qucs syntax test file
* SPICE 2g6 and 3f5 capacitors.
* Pulse test with dc and ac source
* in series with pulse voltage source.
* .subckt S2Q_test4_c p06
* v6 8 0 dc 1v ac 1v pulse(0 1 50ms 1us 1us 100ms 200ms)
  r7 8 p06 10k
  c7 p06 0 1u ic = −1v
.ends
.end

- Vp06.V: **FAIL**; correct dc output = 1V.
- Vp06.v: **PASS**; correct ac waveform.
- Vp06.Vt: **FAIL**; Transient simulation will not run.

NOTE: Vp06.Vt: If **ac 1v** is removed from voltage source statement, v6, the transient analysis gives correct result. Cause unknown.
Figure 11.6: March 22: Test circuit for combined dc, ac and pulse source test

Qucs netlist:

```
# Qucs 0.0.11 /media/hda2/S2Q_test4_prj/S2Q(test4_c).sch

_.Def:S2Q_test4_c_cir _netP06 _ref
_.Def:S2Q_TEST4_C _ref _netP06
Vrect:V6 _net8 _cnet1 U="1" Td="50ms" Tr="1us" TF="1us" TH="0.100002" TL="0.049998"
Vac:V6 _cnet1 _cnet0 U="1V"
Vdc:V6 _cnet0 _ref U="1"
R:R7 _net8 _netP06 R="10k"
C:C7 _netP06 _ref C="1u" V="−1V"
_.Def:End
Sub:X1 _ref _netP06 Type="S2Q_TEST4_C"
_.Def:End

Sub:X1 vp06 gnd Type="S2Q_test4_c_cir"
.DC:DC1 Temp="26.85" reitol="0.001" abstol="1uA" vntol="1mV" saveOPs="no"
MaxIter="150" saveAll="no" convHelper="none" Solver="CroutLU"
.AC:AC1 Type="log" Start="1Hz" Stop="10kHz" Points="400" Noise="no"
.TR:TR1 Type="lin" Start="0" Stop="300ms" Points="300" IntegrationMethod="Gear"
Order="6" InitialStep="0.001µs" MinStep="1e−16" MaxIter="150" reitol="0.01"
abstol="100µA" vntol="100µV" Temp="26.85" LTEreltol="1e−3" LTEabstol="1e−6"
LTEfactor="1" Solver="CroutLU" relaxTSR="no" initialDC="yes" MaxStep="0"
```
E: SPICE 2g6 non-linear capacitor tests.
NO results - Qucs 0.0.11 does not allow non-linear capacitors of the SPICE 2g6 form. Nonlinear capacitors will be added to both Qucs and QUCSCONV sometime in the future when the nonlinear independent voltage and current sources are implemented, see the todo list..

F: SPICE 3f5 tests SPICE code: File S2Q_test4_e.cir
* SPICE to Qucs syntax test file
* SPICE 3f5 semiconductor capacitors.
* DC and AC tests.
* .subckt S2Q_test4_e p01 p02 p03 p04 p05 p06
  v1 1 0 DC 1v AC 1v
  r1 1 p01 10k
  c1 p01 0 1u
  *
  v2 2 0 dc 1v ac 1v
  r3 2 p02 10k
  c2 p02 0 1u ic = 10v
  *
  v3dc 3 0 dc 1v
  v3ac 4 3 ac 1v
  r4 4 p03 10k
  c3 p03 0 1u ic = -10v
  *
  v4dc 5 0 dc 1v
  v4ac 6 5 ac 1v
  r5 6 p04 10k
  c4 p04 0 cmod1 L=10u W=1u
  .model cmod1 C(CJ=50u CJSW=20p NARROW=0.1u)
  *
  v3 7 0 dc 1v ac 1v
  r6 7 p05 10k
  c5 p05 0 cmod1 L=10u W=1u
  *
  v4 8 0 dc 1v ac 1v
  r7 8 p06 10k
  c6 p06 0 cmod2 L=10u
  .model cmod2 C(DEFW=1u CJ=50u CJSW=20p NARROW=0.1u)
  .ends
  .end

Qucs netlist (DC simulation)
# Qucs 0.0.11 /media/hda2/S2Q_test4_prj/S2Q(test4_e).sch

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.Def:S2Q_test4_e_cir _netP01 _netP02 _netP03 _netP04 _netP05 _netP06 _ref
.Def:S2Q_TEST4_E _ref _netP01 _netP02 _netP03 _netP04 _netP05 _netP06
Vac:V4 _net8 _cnet5 U="1V"
Vac:V3 _net7 _cnet4 U="1V"
Vac:V4AC _net6 _cnet3 U="1V"
Vac:V3AC _net4 _cnet2 U="1V"
Vac:V2 _net2 _cnet1 U="1V"
Vac:V1 _net1 _cnet0 U="1V"
Vdc:V1 _cnet0 _ref U="1V"
R:R1 _net1 _netP01 R="10k"
C:C1 _netP01 _ref C="1u"
Vdc:V2 _cnet1 _ref U="1V"
R:R3 _net2 _netP02 R="10k"
C:C2 _netP02 _ref C="1u" V="10V"
Vdc:V3DC _net3 _ref U="1V"
Vdc:V3AC _cnet2 _net3 U="1"
R:R4 _net4 _netP03 R="10k"
C:C3 _netP03 _ref C="1u" V="10V"
Vdc:V4DC _net5 _ref U="1V"
Vdc:V4AC _cnet3 _net5 U="1"
R:R5 _net6 _netP04 R="10k"
C:C4 _netP04 _ref L="10u" W="1u" C="1e-12"
Vdc:V3 _cnet4 _ref U="1V"
R:R6 _net7 _netP05 R="10k"
C:C5 _netP05 _ref L="10u" W="1u" C="1e-12"
Vdc:V4 _cnet5 _ref U="1V"
R:R7 _net8 _netP06 R="10k"
C:C6 _netP06 _ref L="10u" C="1e-12"
.Sub:X1 _ref _netP01 _netP02 _netP03 _netP04 _netP05 _netP06 Type="S2Q_TEST4_E"
.Sub:X1 vp01 vp02 vp03 vp04 vp06 vp07 gnd Type="S2Q_test4_e_cir"
.DC:DC1 Temp="26.85" reltol="0.001" abstol="1pA" vntol="1nV"
saveOPs="no" MaxIter="150" saveAll="no" convHelper="none" Solver="CroutLU"

RESULTS:
line 25: checker error, extraneous property ‘L’ is invalid in ‘C:C4’
line 25: checker error, extraneous property ‘W’ is invalid in ‘C:C4’
line 28: checker error, extraneous property ‘L’ is invalid in ‘C:C5’
line 28: checker error, extraneous property ‘W’ is invalid in ‘C:C5’
line 31: checker error, extraneous property ‘L’ is invalid in ‘C:C6’

Errors in SPICE semiconductor capacitor to Qucs netlist format conversion.

11.3.2 March 25 2007, Simulation tests by Mike Brinson

Code modifications:
• *check_spice.cpp*: Handling capacitor models correctly. Also fixed wrong DC value of sources when neither the DC directive nor an immediate value was given. Stefan Jahn.

A: SPICE 2g6 and 3f5 linear capacitor dc tests:

- Vp01.V: **PASS**: dc output = 0V.
- Vp02.V: **PASS**: dc output = 0V.
- Vp03.V: **PASS**: dc output = 1V.
- Vp04.V: **PASS**: dc output = 1V.
- Vp05.V: **PASS**: dc output = 1V.
- Vp06.V: **PASS**: dc output = 1V.

C: SPICE code: File *S2Q_test4_b.cir*

Further notes on test results:

- SPICE independent voltage sources with DC, AC and transient elements appear to be handled differently by SPICE and Qucs. In a SPICE DC operating point simulation, time domain sources have their DC values set to their value at simulation time equal to zero seconds. However, for time domain pulse source Qucs finds the DC level by integrating it’s waveform over one signal cycle. This results in a DC value of 0.6667V, yielding the DC offset recorded in the original test. In Qucs a generator is added to the Qucs netlist for each of the elements specified in the original SPICE voltage source entry. Hence, it is possible to have upto three voltage sources in series. Figure 11.7 illustrates that the DC offset occurs from a pulse generator placed in series with a DC source on a schematic.

- The same comment concerning SPICE and Qucs differences introduced above applies to the AC component of a SPICE independent voltage source component. In this case there is not a DC offset but because the frequency of the source is NOT included in the SPICE code, Qucs assumes it’s default value to be 1GHz. Hence, in the time domain an AC generator is included in the independent voltage source branch with a frequency of 1GHz. This in turn causes the transient analysis routines to require a very small time step for satisfactory accuracy and hence the simulation takes a long time and appears to hang. SPICE on the other hand considers the AC source to be only applicable to small signal AC analysis and does NOT include it in time domain simulation. Yet another example of the difference between SPICE and Qucs.
Figure 11.7: March 25: DC simulation showing 0.6667V offset

- RECOMMENDATIONS:
  1. Mix DC, AC and time domain source elements in SPICE independent voltage sources with care when converting code to be simulated with Qucs.
  2. When simulating SPICE netlists in the time domain ensure capacitors have their initial condition voltages set to known values. This ensures that the correct DC conditions form the starting point for a transient circuit simulation.

F: SPICE 3f5 tests SPICE code: File S2Q_test4_e.cir
DC simulation test: All outputs PASS with a DC value of 1V.

11.4 References


12 SPICE to Qucs conversion: Test File 5

12.1 Introduction

12.1.1 Title
SPICE 2g6 and 3f5 inductors.

12.1.2 SPICE specification
Format: SPICE 2g61:

- Linear form: LX N+ N- value [ IC = INCOND]
- Nonlinear form: LX N+ N- [POLY] value [L1 [ L2 ....] ] [IC = INCOND ]
- Coupled (mutual) inductors: KX L1 L2 Kvalue

Notes:

1. Characters [ and ] enclose optional items
2. Inductors begin with letter L.
3. X denotes name of inductor
4. N+ and N- are the positive and negative nodes respectively.
5. Value is the inductor value in Henries.
6. L1 and L2 are the names of the two coupled inductors.
7. Kvalue is the coefficient of coupling; 0 < Kvalue and Kvalue < 1.

1See sections 6.2 and 6.3, SPICE 2g6 user’s guide.
8. The “dot” convention is used to denote coupling direction by placing a “dot” on the first node of each inductor.

9. Equations:

Inductors may be nonlinear functions of current, where

\[ L(I) = value + L1 \cdot I + L2 \cdot I^2 + \ldots + Ln \cdot I^n \]

and L1, L2, L3 ........ are the coefficients of a polynomial describing the element value. Also \( n \leq 20 \).

Format: SPICE 3f5:\n
- Linear inductors: \textbf{LX N+ N- value [ IC = INCOND ]}
- Coupled (mutual) inductors: \textbf{KX L1 L2 Kvalue}

Notes: 1 to 8 above.

12.2 Test code

SPICE code: File \texttt{S2Q_test5-_.cir}

```plaintext
* SPICE to Qucs syntax file
* SPICE 2g6 and 3f5 inductance
* DC and AC tests
.subckt S2Q_test5-_.a pol, po2, po3
v1 1 0 dc 1v
l1 1 po1 1mH
r1 po1 0 1k
*
v2 2 0 ac 1v
l2 2 po2 1mH
r2 po2 0 1k
*
v3 3 0 dc 1v ac 1v
l3 3 po3 1mH
r3 po3 0 1k
*
.ends
.end
```

\textsuperscript{2}See sections 3.1.7 and 3.1.8, SPICE 3f6 user’s guide.
SPICE code: File S2Q_test5_b.cir

* SPICE to Qucs syntax file
* SPICE 2g6 and 3f5 inductance
* DC and transient tests
.subckt S2Q_test5_a pol, po2, po3, po4, po5, po6, po7
  v1 1 0 dc 1v
  l1 1 pol lmH ic=0mA
  r1 pol 0 1k
  *
  v2 2 0 dc 0v
  l2 2 po2 lmH ic=-10mA
  r2 po2 0 1k
  *
  v3 3 0 dc 1v
  l3 3 po3 lmH IC=0mA
  r3 po3 0 1k
  *
  v4 4 0 dc 0v pulse(0 1 0.1u 0.1u 0.1u 10u 20u)
  l4 4 po4 lmH ic=0mA
  r4 po4 0 1k
  *
  v5 5 0 dc 1v pulse(0 1 0.1u 0.1u 0.1u 10u 20u)
  l5 5 po5 lmH ic=0mA
  r5 po5 0 1k
  *
  v6 6 0 dc 1v pulse(0 1 0.1u 0.1u 0.1u 10u 20u)
  l6 6 po6 lmH ic=-lmA
  r6 po6 0 1k
  *
  v7 7 0 dc 0v pulse(0 1 0.1u 0.1u 0.1u 10u 20u)
  l7 7 po7 lmH ic=lmA
  r7 po7 0 1k
  *
.ends
.end

SPICE code: File S2Q_test5_c.cir

* SPICE to Qucs syntax file
* SPICE 2g6 and 3f5 mutual inductance
* AC tests
.subckt s2q_test5_c pol po2
  v1 1 0 ac 240
  r1 1 2 10Ohm
  l1 2 0 100mH
  l2 3 0 100mH
SPICE code: File S2Q_test5_d.cir

* SPICE to Qucs syntax file
* SPICE 2g6 and 3f5 mutual inductance
* Transient test
.subckt s2q_test5_c pol
v1 1 0 sin(0 240 50)
rl 1 2 1Ohm
l1 2 0 100mH
l2 3 0 100mH
k23 l1 l2 0.999
r2 3 pol 1Ohm
rl pol 0 150
.ends
.end

SPICE code: File S2Q_test5_e.cir

* SPICE to Qucs syntax file
* SPICE 2g6 and 3f5 mutual inductance
* Transient test – two sets of coupling
.subckt s2q_test5_c pol pol
v1 1 0 sin(0 240 50)
rl 1 2 1Ohm
l1 2 0 100mH
l2 3 0 100mH
l3 0 4 100mH
k12 l1 l2 0.999
k13 l1 l3 0.999
k23 l2 l3 0.999
r2 3 pol 1Ohm
rl1 pol 0 150
r3 4 pol 2 1Ohm
rl2 pol 2 0 150
.ends
.end

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12.3 History of simulation results

12.3.1 April 17 2007, Simulation tests by Mike Brinson

Summary:

- File s2q_5.a: All DC and AC results correct.
- File s2q_5.b: All DC and transient results correct. NOTE: Outputs po4.V, po5.V, po6.V and po7.V have a value of 0.513 added to the DC source values. This corresponds to the DC value of the pulse sources. Changing, for example, time parameter TD changes this value.
- File s2q_5.c: All results appear to be correct.
- File s2Q_5.d: All results appear to be correct.
- File s2q_5.e: All results appear to be correct.
- Inductive coupled networks with more than three coupling coefficients have not been tested.
- SPICE 2g6 non-linear inductors have not been tested. Future implementation of Qucs nonlinear controlled sources will allow simulation of current dependent inductors.
Figure 12.1: April 17: Inductor DC and AC test schematic for file s2q_5_a.cir

Figure 12.2: April 17: Inductor DC and AC tests results for file s2q_5_a.cir
# Qucs 0.0.12 /media/hda2/S2Q_test5_prj/test_s2q_5_a.sch

```
.Def:s2q_test5_a_cir _netPO1 _netPO2 _netPO3 _ref
.Def:S2Q_TEST5_A _ref _netPO1 _netPO2 _netPO3
Vac:V3 _net3 _cnet1 U="1V"
Vac:V2 _net2 _cnet0 U="1V"
Vdc:V1 _net1 _ref U="1V"
L:L1 _net1 _netPO1 L="1mH"
R:R1 _netPO1 _ref R="1k"
Vdc:V2 _cnet0 _ref U="0"
L:L2 _net2 _netPO2 L="1mH"
R:R2 _netPO2 _ref R="1k"
Vdc:V3 _cnet1 _ref U="1V"
L:L3 _net3 _netPO3 L="1mH"
R:R3 _netPO3 _ref R="1k"
.Def:End
Sub:X1 _ref _netPO1 _netPO2 _netPO3 Type="S2Q_TEST5_A"
.Def:End
Sub:X1 P01 P02 P03 gnd Type="s2q_test5_a_cir"
.AC:AC1 Type="log" Start="1 Hz" Stop="100 kHz" Points="100" Noise="no"
.DC:DC1 Temp="26.85" reltol="0.001" abstol="1 pA" vntol="1 uV"
saveOPs="no" MaxIter="150" saveAll="no" convHelper="none" Solver="CroutLU"
```

Figure 12.3: April 17: s2q_5_a Qucs netlist

Figure 12.4: April 17: Inductor DC and transient test schematic for file s2q_5_b.cir
Figure 12.5: April 17: Inductor DC and transient tests results for file s2q_5_b.cir
# Qucs 0.0.12 /media/hda2/S2Q_test5_prj/test_s2q_5_b.sch

```
.Def:s2q_test5_b_cir _netPO1 _netPO2 _netPO3 _netPO4 _netPO5 _netPO6
.NetPO7 _ref
.Def:S2Q_TEST5_A _ref _netPO1 _netPO2 _netPO3 _netPO4 _netPO5 _netPO6
.NetPO7
Vrect:V7 _net7 _cnet3 U="1" Td="0.1u" Tr="0.1u" Tf="0.1u" TH="1.02e-05"
TL="9.7e-06"
Vrect:V6 _net6 _cnet2 U="1" Td="0.1u" Tr="0.1u" Tf="0.1u" TH="1.02e-05"
TL="9.7e-06"
Vrect:V5 _net5 _cnet1 U="1" Td="0.1u" Tr="0.1u" Tf="0.1u" TH="1.02e-05"
TL="9.7e-06"
Vrect:V4 _net4 _cnet0 U="1" Td="0.1u" Tr="0.1u" Tf="0.1u" TH="1.02e-05"
TL="9.7e-06"
Vdc:V1 _net1 _ref U="1V"
L:L1 _net1 _netPO1 L="1mH" I="0mA"
R:R1 _netPO1 _ref R="1k"
Vdc:V2 _net2 _ref U="0V"
L:L2 _net2 _netPO2 L="1mH" I="-10mA"
R:R2 _netPO2 _ref R="1k"
Vdc:V3 _net3 _ref U="1V"
L:L3 _net3 _netPO3 L="1mH" I="0mA"
R:R3 _netPO3 _ref R="1k"
Vdc:V4 _cnet0 _ref U="0"
L:L4 _net4 _netPO4 L="1mH" I="0mA"
R:R4 _netPO4 _ref R="1k"
Vdc:V5 _cnet1 _ref U="1"
L:L5 _net5 _netPO5 L="1mH" I="0mA"
R:R5 _netPO5 _ref R="1k"
Vdc:V6 _cnet2 _ref U="1"
L:L6 _net6 _netPO6 L="1mH" I="-1mA"
R:R6 _netPO6 _ref R="1k"
Vdc:V7 _cnet3 _ref U="0"
L:L7 _net7 _netPO7 L="1mH" I="1mA"
R:R7 _netPO7 _ref R="1k"
.Def:End
Sub:X1 _ref _netPO1 _netPO2 _netPO3 _netPO4 _netPO5 _netPO6 _netPO7
Type="S2Q_TEST5_A"
.Def:End

.DC:DC1 Temp="26.85" reltol="0.001" abstol="1.nA" vntol="1.nV" saveOPs="no"
MaxIter="150" saveAll="no" convHelper="none" Solver="CroutLU"
.TR:TR1 Type="lin" Start="0" Stop="21u" Points="100" IntegrationMethod="Gear"
Order="6" InitialStep="1.ns" MinStep="1e-16" MaxIter="150" reltol="0.01"
abstol="100.nA" vntol="100.nV" Temp="26.85" LTEreltol="1e-3"
LTEabstol="1e-6" LTEfactor="1" Solver="CroutLU" relaxTSR="no"
initialDC="yes" MaxStep="0"
Sub:X1 po1 po2 po3 po4 po5 po6 po7 gnd Type="s2q_test5_b_cir"
```

Figure 12.6: April 17: s2q_5_b Qucs netlist
Figure 12.7: April 17: Mutual inductance AC test schematic for file s2q_5_c.cir

```
Figure 12.8: April 17: Mutual inductance tests results for file s2q_5_c.cir
```

```plaintext
Equation
Eqn1
vpo1=abs(po1.v)
phase_vpo1=phase(po1.v)
phase_vpo2=rad2deg(unwrap(angle(po2.v)))
real_vpo1=real(po1.v)
real_vpo2=real(po2.v)
imag_vpo1=imag(po1.v)
imag_vpo2=imag(po2.v)
```
.Def:s2q_test5_c_cir _netPO1 _netPO2 _ref
  .Def:S2Q_TEST5_C _ref _netPO1 _netPO2
  L:K231 _cnet3 _ref L="0.0999"
  L:K23 _cnet1 _ref L="0.0999"
  Vac:V1 _net1 _cnet0 U="240"
  Vdc:V1 _cnet0 _ref U="0"
  R:R1 _net1 _net2 R="10Ohm"
  L:L1 _net2 _cnet1 L="0.0001"
  L:L2 _net3 _cnet2 L="0.0001"
  Tr:K23 _cnet1 _cnet2 _ref _ref T="1"
  R:R2 _net3 _netPO1 R="10Ohm"
  R:RL _netPO1 _ref R="150"
  R:R11 _net1 _net21 R="/1Ohm"
  L:L11 _net21 _cnet3 L="0.0001"
  L:L21 _ref _cnet4 L="0.0001"
  Tr:K231 _cnet3 _cnet4 _net31 _ref T="1"
  R:R21 _net31 _netPO2 R="10Ohm"
  R:RL1 _netPO2 _ref R="150"
  .Def:End
  Sub:X1 _ref _netPO1 _netPO2 Type="S2Q_TEST5_C"
  .Def:End
  .DC:DC1 Temp="26.85" reltol="0.001" abstol="1\,\mu A" vntol="1\,\mu V" saveOPs="no" MaxIter="150" saveAll="no" convHelper="none" Solver="CroutLU"
  .AC:AC1 Type="log" Start="1\,Hz" Stop="10\,MHz" Points="100" Noise="no"
  Sub:X1 pol po2 gnd Type="s2q_test5_c_cir"
  Eqn:Eqn1 vpo1="abs ( po1.v )" phase_vpo1="phase ( po1.v )"
  phase_vpo2="rad2deg ( unwrap ( angle ( po2.v ) ) )" vpo2="abs ( po2.v )"
  real_vpo1="real ( po1.v )" real_vpo2="real ( po2.v )" imag_vpo1="imag ( po1.v )"
  imag_vpo2="imag ( po2.v )" Export="yes"

Figure 12.9: April 17: s2q_5_c Qucs netlist
Figure 12.10: April 17: Mutual inductance transient test schematic for file s2q_5_d.cir

Figure 12.11: April 17: Mutual inductance transient tests results for file s2q_5_d.cir
Def: s2q_test5_d_cir_netPO1_ref
.Def: S2Q_TEST5_C_ref_netPO1
L: K23 _cnet1_ref L="0.0999"
Vac: V1 _net1_cnet0 U="240" f="50" Phase="0" Theta="0"
Vdc: V1 _cnet0_ref t="0"
R: R1 _net1_net2 R="1Ohm"
L: L1 _net2_cnet1 L="0.0001"
L: L2 _net3_cnet2 L="0.0001"
Tr: K23 _cnet1_cnet2_ref_ref T="1"
R: R2 _net3_netPO1 R="1Ohm"
R: RL _netPO1_ref R="150"
.Def: End
Sub: X1_ref_netPO1 Type="S2Q_TEST5_C"
.Def: End

Sub: X1 vp01 gnd Type="s2q_test5_d_cir"
.DC: DC1 Temp="26.85" reltol="0.001" abstol="1pA"
vntol="1uV" saveOPs="no" MaxIter="150" saveAll="no"
convHelper="none" Solver="CroutLU"
.TR: TRI Type="lin" Start="0" Stop="100 ms" Points="1000"
IntegrationMethod="Trapezoidal" Order="2" InitialStep="1ns"
MinStep="1e-16" MaxIter="150" reltol="0.001" abstol="1pA"
vntol="1uV" Temp="26.85" LTEreltol="1e-3" LTEabstol="1e-6"
LTEfactor="1" Solver="CroutLU" relaxTSR="no" initialDC="yes" MaxStep="0"

Figure 12.12: April 17: s2q_5_d Qucs netlist
Figure 12.13: April 17: Mutual inductance transient test schematic for file s2q_5_e.cir

<table>
<thead>
<tr>
<th>number</th>
<th>po1.V</th>
<th>po2.V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 12.14: April 17: Mutual inductance transient tests results for file s2q_5_e.cir
```plaintext
# Qucs 0.0.12 /media/hda2/S2Q_test5_prj/test_s2q_5_e.sch

.Def:s2q_test5_e_cir netPO1 netPO2 ref
.Def:S2Q_TEST5_C ref netPO1 netPO2
Vac:V1 _net1 _cnet0 U="240" f="50" Phase="-0" Theta="0"
Vdc:V1 _cnet0 ref U="0"
R:R1 _net1 _net2 R="1Ohm"
MUT2:K12K13K23 _net2 ref _net4 _ref _net3 _ref L1="0.1" L2="0.1"
L3="0.1" k12="0.999" k13="0.999" k23="0.999"
R:R2 _net3 _netPO1 R="1Ohm"
R:RL1 _netPO1 ref R="150"
R:R3 _net4 _netPO2 R="1Ohm"
R:RL2 _netPO2 ref R="150"
.Def:End
Sub:X1 _ref _netPO1 _netPO2 Type="S2Q_TEST5_C"
.Def:End

Sub:X1 po1 po2 gnd Type="s2q_test5_e_cir"
.DC:DC1 Temp="26.85" reltol="0.001" abstol="1µA" vntol="1µV" saveOPs="no"
MaxIter="150" saveAll="no" convHelper="none" Solver="CroutLU"
.TR:TR1 Type="lin" Start="0" Stop="100µs" Points="1000"
IntegrationMethod="Trapezoidal" Order="2" InitialStep="1µs"
MinStep="1e-16" MaxIter="150" reltol="0.001" abstol="1µA" vntol="1µV"
Temp="26.85" LTEreltol="1e-3" LTEabstol="1e-6" LTEfactor="1"
Solver="CroutLU" relaxTSR="no" initialDC="yes" MaxStep="0"

Figure 12.15: April 17: s2q_5_e Qucs netlist
```

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13 A Curtice level 1 MESFET model

13.1 Introduction

The Metal and Semiconductor FET (MESFET) is a Schottky-barrier gate FET made from gallium arsenide. It is popular for high frequency applications because of its high electron mobility. The device was developed by Walter R. Curtice\(^1\) in 1980 at the RCA Laboratory in Princeton, New Jersey, USA. The MESFET model presented below is based on a Qucs equation defined device (EDD) which functions as a Curtice level 1 MESFET model with interelectrode capacitances. Basic temperature effects are also included.

13.2 Qucs EDD model for the Curtice MESFET

Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>RG</td>
<td>(R_G)</td>
<td>external gate resistance</td>
<td>(\Omega)</td>
<td>1m</td>
</tr>
<tr>
<td>RD</td>
<td>(R_D)</td>
<td>external drain resistance</td>
<td>(\Omega)</td>
<td>1m</td>
</tr>
<tr>
<td>RS</td>
<td>(R_S)</td>
<td>external source resistance</td>
<td>(\Omega)</td>
<td>1m</td>
</tr>
<tr>
<td>VBR</td>
<td>(V_{DR})</td>
<td>GS breakdown voltage</td>
<td>V</td>
<td>(10^{10})</td>
</tr>
<tr>
<td>LG</td>
<td>(L_G)</td>
<td>external gate lead inductance</td>
<td>H</td>
<td>0</td>
</tr>
<tr>
<td>LD</td>
<td>(L_D)</td>
<td>external drain lead inductance</td>
<td>H</td>
<td>0</td>
</tr>
<tr>
<td>LS</td>
<td>(L_S)</td>
<td>external source lead inductance</td>
<td>H</td>
<td>0</td>
</tr>
<tr>
<td>Is</td>
<td>(I_S)</td>
<td>diode saturation current</td>
<td>A</td>
<td>10f</td>
</tr>
<tr>
<td>N</td>
<td>(N)</td>
<td>diode emission coefficient</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>XTI</td>
<td>(X_{TI})</td>
<td>diode saturation current temperature coefficient</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>EG</td>
<td>(E_G)</td>
<td>diode energy gap</td>
<td>eV</td>
<td>1.11</td>
</tr>
<tr>
<td>TAU</td>
<td>(\tau)</td>
<td>internal time delay from drain to source</td>
<td>s</td>
<td>10p</td>
</tr>
<tr>
<td>RIN</td>
<td>(R_{IN})</td>
<td>series resistance to CGS</td>
<td>(\Omega)</td>
<td>1m</td>
</tr>
<tr>
<td>CGS</td>
<td>(C_{GS})</td>
<td>interelectrode gate-source bias-independent</td>
<td>F</td>
<td>300f</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>CGD</td>
<td>$C_{GD}$</td>
<td>capacitance interelectrode gate-drain bias-independent capacitance</td>
<td>F</td>
<td>300f</td>
</tr>
<tr>
<td>CDS</td>
<td>$C_{DS}$</td>
<td>capacitance interelectrode drain-source bias-independent capacitance</td>
<td>F</td>
<td>300f</td>
</tr>
<tr>
<td>Tnom</td>
<td>$T_{NOM}$</td>
<td>device parameter measurement temperature</td>
<td>°C</td>
<td>27</td>
</tr>
<tr>
<td>Temp</td>
<td>$T$</td>
<td>device temperature</td>
<td>°C</td>
<td>27</td>
</tr>
<tr>
<td>Alpha</td>
<td>$\alpha$</td>
<td>coefficient of $V_{ds}$ in tanh function for quadratic model</td>
<td>1/V</td>
<td>0.8</td>
</tr>
<tr>
<td>Beta</td>
<td>$\beta$</td>
<td>transconductance parameter</td>
<td>A/V^2</td>
<td>3m</td>
</tr>
<tr>
<td>Lambda</td>
<td>$\lambda$</td>
<td>channel length modulation parameter for quadratic model</td>
<td>1/V</td>
<td>40m</td>
</tr>
<tr>
<td>VTO</td>
<td>$V_{TO}$</td>
<td>quadratic model gate threshold voltage</td>
<td>V</td>
<td>−6</td>
</tr>
</tbody>
</table>
Figure 13.1: A Qucs EDD model for the Curtice MESFET
13.3 The MESFET equations

- DC characteristics
  1. for \((V_{GS} < -V_{BR} + 50 \cdot V_T)\)
    \[
    I_{GS} = -I_S(T) \cdot \left(1 + \exp\left(-\frac{V_{BR} + V_{GS}}{V_T}\right)\right) + G_{MIN} \cdot V_{GS} \quad (13.1)
    \]
  2. for \((V_{GS} \geq -V_{BR} + 50 \cdot V_T)\) and \((V_{GS} < -5 \cdot V_T)\)
    \[
    I_{GS} = -I_S(T) + G_{MIN} \cdot V_{GS} \quad (13.2)
    \]
  3. for \((V_{GS} \geq -5 \cdot V_T)\)
    \[
    I_{GS} = I_S(T) \cdot \left(\exp\left(\frac{V_{GS}}{V_{N} \cdot V_T}\right) - 1\right) + G_{MIN} \cdot V_{GS} \quad (13.3)
    \]
  4. for \((V_{GS} - V_{TO}) > 0\)
    \[
    I_{DS} = \beta \cdot (V_{GS} - V_{TO})^2 \cdot \left(1 + \lambda \cdot V_{DS}\right) \cdot \tanh(\alpha \cdot V_{DS}) \quad (13.4)
    \]

Where

\[
I_S(T) = I_S \cdot \exp\left(\frac{X_{TI}}{N} \cdot \ln(TR) - \left(E_G/N/V_T\right) \cdot (1 - TR)\right) \quad (13.5)
\]

\[
TR = \frac{TK}{TnK} \quad \text{and} \quad TK = T + 273.15, \quad TnK = T_{NOM} + 273.15 \quad (13.6)
\]

- MESFET charge equations
  1. \(Q_{GS} = C_{GS} \cdot V_{GS}\) \quad (13.7)
  2. \(Q_{GD} = C_{GD} \cdot V_{GD}\) \quad (13.8)
  3. \(Q_{DS} = C_{DS} \cdot V_{DS} + \tau \cdot I_{DS}\) \quad (13.9)
13.4 Test circuits and simulation results

Figure 13.2: DC test circuit and Id-Vds characteristics
Figure 13.3: DC test circuit and Id-Vgs characteristics
Figure 13.4: DC test circuit and Ig-Vgs characteristics
Figure 13.5: S parameter test circuit and characteristics