Qucs

A Report

Verilog-A compact device models for GaAs MESFETs

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Introduction

A previous Qucs Report\(^1\) described a MESFET model based on an equation defined device (EDD) representation of the level 1 Curtice model. This model evolved as a test example during the initial Qucs EDD development phase. Today the EDD model is popular amongst Qucs users as either a powerful non-linear component in its own right or as the basis of a component prototyping system for constructing compact Verilog-A device models, translated with ADMS to C++ code, compiled to object code and finally linked to the main body of the Qucs program code. Over the last year the Qucs development team has invested a significant amount of time improving both EDD prototyping and Verilog-A compact device/circuit model development, making the development process more transparent to anyone interested in trying their hand at model construction. One branch of the current Qucs modelling activities is concentrating on adding new models which fill in some of the gaps in the Qucs released model lists. One such model in this category is the GaAs MESFET. This report outlines the background and mathematical basis for a number of MESFET models. These have been coded in Verilog-A and tested using recent Qucs CVS code. They will be included in the next full release of Qucs.

The GaAs MESFET

The metal-semiconductor FET (MESFET) is a Schottky-barrier gate FET which is normally made from Gallium Arsenide. It is a popular device for high frequency applications because of its high electron mobility and usable gain at microwave frequencies. An early simulation model for the MESFET device was developed by Walter R. Curtice\(^2\) in 1980 at the RCA Laboratory in Princeton, New Jersey, USA. Since Curtice published his original MEFET model a number of authors have contributed improvements to the basic model, including for example Statz et. al. (Raytheon)\(^3\) and TriQuint Semiconductor Inc.\(^4\). These models form the basis of the Qucs MESFET model described in this report.

\(^1\)M. Brinson and S. Jahn, Qucs: Compact device- circuit macromodel specification; A Curtice level 1 MESFET model, http://qucs.sourceforge.net/docs.html
\(^4\)For example, D.H. Smith, TOM-2: An improved Model for GaAs MESFETs, TriQuint Report, TriQuint Semiconductor, Inc Feb. 27, 1995 (11 pages).
# The Qucs MESFET model

## Parameters

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<tr>
<th>Name</th>
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Where parameter LEVEL selects a MESFET model listed in Table 2.

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Table 2: Qucs MESFET model types

MESFET gate current equations can be selected by setting parameters ILEVELS and ILEVELD. Table 3 lists the available options.

MESFET charge equations can be selected by setting parameters QLEVELS, QLEVELD and QLEVELDS. Table 4 lists the available options. Although it
is possible to mix the five basic MESFET models with different gate current and charge equation models the common default models are the ones listed in Table 5.

![Image](image.png)

Table 3: Qucs MESFET gate current model types

Table 4: Qucs MESFET charge equation types

Table 5: Qucs MESFET default selection parameters

The Qucs MESFET simulation model

The large signal equivalent circuit for the Qucs MESFET model is illustrated in Fig. 1. The currents flowing in each of the circuit branches are given by the Verilog-A code fragment shown in Fig. 1. The Verilog-A HDL code for the entire Qucs MESFET model is available from the Qucs CVS archive[^5]. In order to simulate

the operation of an MESFET, equations based on the physical operation of the
device are required for all the current contribution components in Fig. 1. These
equations are presented in the remaining sections of this report. Examples are also
introduced to demonstrate the simulation performance of each model.

**MESFET gate current equations**

- **ILEVELS = 0**: \( I_{gs} = 0 \text{ A} \)
- **ILEVELS = 1**: if \((V(b1) > Vbi)\)

\[
I_{gs} = \frac{V(b1) - Vbi}{Rf} 
\]

else

\[
I_{gs} = -Area \cdot Is + GMIN \cdot V(b1)
\]

- **ILEVELS = 2**: if \((V(b1) > Vbi)\)

\[
I_{gs1} = \frac{V(b1) - Vbi}{Rf} 
\]

else

\[
I_{gs1} = -Area \cdot Is + GMIN \cdot V(b1)
\]

if \(V(b1) < -Bv)\)

\[
I_{gs2} = \frac{V(b1) - Vbi}{R1} 
\]

\[
I_{gs} = I_{gs1} + I_{gs2}
\]

- **ILEVELS = 3**: if \((V(b1) > Vbi)\)

\[
I_{gs} = Is_{T2} \cdot \left\{ \lim_{x \to \infty} \left( \frac{V(b1)}{N \cdot Vt_{T2}} \right) - 1.0 \right\} + GMIN \cdot V(b1)
\]

else

\[
I_{gs} = -Is_{T2} + GMIN \cdot V(b1)
\]

- **ILEVELS = 4**: if \((V(b1) > -5 \cdot N \cdot Vt_{T2})\)

\[
I_{gs1} = Area \cdot Is_{T2} \cdot \left\{ \lim_{x \to \infty} \left( \frac{V(b1)}{N \cdot Vt_{T2}} \right) - 1.0 \right\} + GMIN \cdot V(b1)
\]

else

\[
I_{gs1} = 0
\]

if \((-Bv < V(b1)) \) and \((V(b1) < -5 \cdot N \cdot Vt_{T2}))\)

\[
I_{gs2} = -Area \cdot Is_{T2} + GMIN \cdot V(b1)
\]
Figure 1: Qucs MESFET symbol and large signal equivalent circuit

\[
I_{gs2} = 0
\]

if \((V(b1) == -Bv)\)

\[
I_{gs3} = -I_{bv}
\] \hspace{1cm} (8)

else

\[
I_{gs3} = 0
\]

if \((V(b1) < -Bv)\)

\[
I_{gs4} = -\text{Area} \cdot I_{s \_T2} \cdot \left\{ \lim_{x \to -\infty} \exp \left( -\frac{(Bv + V(b1))}{V_{t \_T2}} \right) - 1.0 + \frac{Bv}{V_{t \_T2}} \right\}
\] \hspace{1cm} (9)

else

\[
I_{gs} = I_{gs1} + I_{gs2} + I_{gs3} + I_{gs4}
\] \hspace{1cm} (10)

Where \(x\_T2\) indicates the values of temperature dependent parameters at circuit temperature \(T2\). See later sections of this report for more details. The gate to drain current equations are identical except \(I_{gs}\) is replaced by \(I_{gd}\), \(I_{gsx}\) by \(I_{gdx}\), and \(V(b1)\) by \(V(b2)\). More details can be found in the Verilog-A listing given in the Qucs CVS code held at the Qucs Sourceforge site.

**MESFET charge equations QLEVELS 0 to 2**

- QLEVELS = 0: [NO charge]:

---
\[ Q_{gs} = 0 \]  \hspace{1cm} (11)

- **QLEVELES = 1**: [Fixed capacitor charge]
  \[ Q_{gs} = \text{Area} \cdot C_{gs} \cdot V(b4) \]  \hspace{1cm} (12)

- **QLEVELES = 2**: [Diode charge]
  if \( V(b4) < (F_c \cdot V_{bi}) \)
  \[ Q_{gs1} = \frac{C_{gs \cdot T2} \cdot V_{bi \cdot T2}}{(1 - M)} \cdot \left\{ 1 - \left( 1 - \frac{V(b4)}{V_{bi \cdot T2}} \right)^{1-M} \right\} \]  \hspace{1cm} (13)
  if \( V(b4) >= (F_c \cdot V_{bi}) \)
  \[ H1 = \frac{M}{2 \cdot V_{bi \cdot T2}} \cdot (V(b4) \cdot V(b4) - (F_c \cdot F_c \cdot V_{bi \cdot T2} \cdot V_{bi \cdot T2})) \]  \hspace{1cm} (14)
  \[ Q_{gs2} = C_{gs \cdot T2} \cdot \left[ F1 + \frac{1}{F2} \cdot \left\{ F3 \cdot (V(b4) - F_c \cdot V_{bi \cdot T2}) + H1 \right\} \right] \]  \hspace{1cm} (15)

Where,
\[ F1 = \frac{V_{bi \cdot T2}}{1 - M} \cdot \left\{ 1 - (1 - F_c)^{1-M} \right\}, \]  \hspace{1cm} (16)
\[ F2 = (1 - F_c)^{1+M}, \]  \hspace{1cm} (17)
and
\[ F3 = 1 - F_c \cdot (1 + M). \]  \hspace{1cm} (18)

Again \( xx \_T2 \) indicates the values of temperature dependent parameters at circuit temperature \( T2 \). See a later section of this report for more details. The gate to drain charge equations (types 0 to 2) are identical except \( Q_{gs} \) is replaced by \( Q_{gd} \), \( Q_{gsx} \) by \( Q_{gdx} \), and \( V(b4) \) by \( V(b6) \). More details can be found in the Qucs CVS code held at the Qucs Sourceforge site.

**MESFET charge equations QLEVELDS 0 to 2**

- **QLEVELES = 0**: [NO charge]:
  \[ Q_{ds} = 0 \]  \hspace{1cm} (19)
• QLEVELDS = 1: [Fixed capacitor charge]

\[ Q_{ds} = \text{Area} \cdot C_{ds} \cdot V(b3) \]  
(20)

• QLEVELS = 2: [Fixed capacitor plus transit charge]

\[ Q_{ds} = \text{Area} \cdot C_{ds} \cdot V(b3) + \tau \cdot I_{ds} \]  
(21)

Curtice hyperbolic tangent model: LEVEL = 1

if \((V(b1) - V_{to_T2}) > 0\)

\[ I_{ds} = \beta_2 \cdot (V(b1) - V_{to_T2})^2 \cdot \left\{ 1 + \lambda \cdot V(b3) \right\} \cdot \tanh(\alpha \cdot V(b3)) \]  
(22)

else \(I_{ds} = 0\).
Figure 2: Curtice LEVEL 1 DC test circuit and Ids-Vds characteristics
Figure 3: Curtice LEVEL 1 DC test circuit and Ids-Vgs characteristics
Figure 4: Curtice LEVEL 1 DC test circuit and Ig-Vgs characteristics
Figure 5: Curtice LEVEL 1 S parameter test circuit and characteristics
Curtice hyperbolic tangent model with subthreshold modification: LEVEL = 2

\[ I_{ds} = \text{Beta}_T V_f \cdot \{1 + \text{Lambda} \cdot V(b3)\} \cdot \tanh(\text{Alpha} \cdot V(b3)) \]  
(23)

Where

\[ V_f = \frac{1}{\text{Ah}} \cdot \ln \{1 + \exp (\text{Ah} \cdot (V(b1) - V_{toT}))\} \]  
(24)

and

\[ \text{Ah} = \frac{1}{2 \cdot N_{sc \cdot V_{tT}}} \]  
(25)

When \( V(b2) > V_{toT} \), \( V_f \rightarrow V(b2) - V_{toT} \). Otherwise, \( V_f \) approaches zero asymptotically. This modification to the basic Curtice model provides an improved match to channel gradual pinch-off and MESFET subthreshold conduction.
Figure 6: Curtice LEVEL 2 DC test circuit and Ids-Vgs characteristics illustrating subthreshold conduction modification
Statz et al. (Raytheon) model: LEVEL = 3

if \( (V(b1) - V_{to\_T2}) > 0 \)
if \( (0 < V(b3)) \) and \( (V(b3) < \frac{3}{\alpha}) \)
begin
\[
H1 = \frac{1 - \left\{1 - \frac{\alpha \cdot V(b3)}{3}\right\}^3}{1 + B \cdot (V(b1) - V_{to\_T2})}
\]  
\( Id_s = Beta_{\_T2} \cdot \{1 + \lambda \cdot V(b3)\} \cdot (V(b1) - V_{to\_T2})^2 \cdot H1 \)  
end
if \( (V(b3) > \frac{3}{\alpha}) \)
\( Id_s = Beta_{\_T2} \cdot \{1 + \lambda \cdot V(b3)\} \cdot (V(b1) - V_{to\_T2})^2 \)
else \( Id_s = 0. \)

MESFET charge equations QLEVELS = 3 and QLEVELED = 3

QLEVELS = 3 : Statz et. al. charge equations

\[
V_{max} = \min(Fc \cdot V_{bi}, V_{max}) \]  
\[
V_{eff1} = 0.5 \cdot \left\{V(b4) + V(b6) + \sqrt{(V(b6) - V(b4))^2 + V_{\delta1}^2}\right\} \]  
\[
V_{new} = 0.5 \cdot \left\{V_{\_eff1} + V_{to\_T2} + \sqrt{(V_{\_eff1} - V_{to\_T2})^2 + V_{\delta2}^2}\right\} \]
if \( (V_{new} > V_{max}) \)
\[
Qgs = Cgs_{\_T2} \cdot \left\{2 \cdot V_{bi\_T2} \cdot \left(1 - \sqrt{1 - \frac{V_{max}}{V_{bi\_T2}}} + \frac{V_{new} - V_{max}}{\sqrt{1 - \frac{V_{max}}{V_{bi\_T2}}}}\right)\right\} \]  
if \( (V_{new} \leq V_{max}) \)
\[
Qgs = Cgs_{\_T2} \cdot 2 \cdot V_{bi\_T2} \cdot \left\{1 - \sqrt{1 - \frac{V_{new}}{V_{bi\_T2}}}\right\} \]
Figure 7: Statz et. al. LEVEL 3 DC test circuit and Ids-Vds characteristics

QLEVELD = 3 : Statz et. al. charge equations

\[
V_{eff2} = 0.5 \cdot \left\{ V(b4) + V(b6) - \sqrt{(V(b4) - V(b6))^2 + V_{delta1}^2} \right\} \quad (34)
\]

\[
Q_{ds} = C_{gd} \cdot V_{eff2} \quad (35)
\]

During simulation gate charge must be partitioned between gate-source and gate-drain branches. The Qucs implementation of the Statz et. al. MESFET model uses the procedure adopted by Divehar \(^6\).

Figure 8: Statz et. al. LEVEL 3 DC test circuit and Ids-Vgs characteristics
Figure 9: Statz et. al. LEVEL 3 DC test circuit and Ig-Vgs characteristics
Figure 10: Statz et. al. LEVEL 3 S parameter test circuit and characteristics
TriQuint Semiconductor TOM 1 model: LEVEL = 4

if \((V(b1) - V_{to\_T2}) > 0\)
  if \((0 < V(b3))\) and \((V(b3) < \frac{3}{\text{Alpha}})\)
    begin
      \(Ids_1 = \left\{ Beta_{\_T2} \cdot (V(b1) - V_{to\_T2})^{Qp} \right\} \cdot \left\{ 1 - \left( 1 - \frac{\text{Alpha} \cdot V(b3)}{3} \right)^3 \right\} \) \hspace{1cm} (36)

      \(Ids = \frac{Ids_1 \cdot \{ 1 + \text{Lambda} \cdot V(b3) \}}{1 + \Delta \cdot V(b3) \cdot Ids_1} \) \hspace{1cm} (37)

    end
  end if

if \((V(b3) > \frac{3}{\text{Alpha}})\)

    \(Ids_1 = Beta_{\_T2} \cdot (V(b1) - V_{to\_T2})^{Qp} \) \hspace{1cm} (38)

    \(Ids = \frac{Ids_1 \cdot \{ 1 + \text{Lambda} \cdot V(b3) \}}{1 + \Delta \cdot V(b3) \cdot Ids_1} \) \hspace{1cm} (39)

else \(Ids = 0.\)
Figure 11: TOM1 LEVEL 4 DC test circuit and Ids-Vds characteristics

Figure 12: TOM1 LEVEL 4 DC test circuit and Ids-Vgs characteristics
Figure 13: TOM1 LEVEL 4 DC test circuit and Ig-Vgs characteristics
Figure 14: TOM1 LEVEL 4 S parameter test circuit and characteristics
TriQuint Semiconductor TOM 2 model: LEVEL = 5

if \((V(b1) - V_{to\_T2}) > 0\)
begin

\[ Nst = Ng + Nd \cdot V(b3) \] (40)

if \((Nst < 1.0)\) \(Nst = 1.0\)

\[ V_{st} = Nst \cdot V_{t\_T2} \] (41)

\[ V_g = Q_p \cdot V_{st} \cdot \ln \left( \exp \left\{ \frac{V(b1) - V_{to\_T2} + Gamma_{T2} \cdot V(b3)}{Q_p \cdot V_{st}} \right\} + 1 \right) \] (42)

\[ Al = Alpha_{T2} \cdot V(b3) \] (43)

\[ F_d = \frac{Al}{\sqrt{1 + Al \cdot Al}} \] (44)

\[ I_{ds1} = Beta_{T2} \cdot V_{gQp} \cdot F_d \] (45)

\[ I_{ds} = I_{ds1} \cdot \frac{1 + Lambda \cdot V(b3)}{1 + Delta \cdot V(b3) \cdot I_{ds1}} \] (46)

end

else \(I_{ds} = 0\)
Figure 15: TOM2 LEVEL 5 DC test circuit and Ids-Vds characteristics
Figure 16: TOM2 LEVEL 5 DC test circuit and Ids-Vgs characteristics
Figure 17: TOM2 LEVEL 5 DC test circuit and Ig-Vgs characteristics
Figure 18: TOM2 LEVEL 5 S parameter test circuit and characteristics
Temperature scaling relations

\[ T_1 = T_{nom} + 273.15; \]
\[ T_2 = Temp + 273.15; \]
\[ Tr = T_2 / T_1; \]
\[ con1 = \text{pow}(Tr, 1.5); \]
\[ Rg_{T2} = Rg \times (1 + Rgtc \times (T_2 - T_1)); \]
\[ Rd_{T2} = Rd \times (1 + Rdtc \times (T_2 - T_1)); \]
\[ Rs_{T2} = Rs \times (1 + Rstc \times (T_2 - T_1)); \]
\[ Beta_{T2} = \text{Area} \times Beta \times \text{pow}(1.01, Betatc \times (T_2 - T_1)); \]
\[ Vt_{T2} = Vt; \]
\[ Eg_{T1} = Eg - 7.02e-4 \times T_1 \times T_1 / (1108 + T_1); \]
\[ Eg_{T2} = Eg - 7.02e-4 \times T_2 \times T_2 / (1108 + T_2); \]
\[ Vbi_{T2} = (Tr \times Vbi) - (2 \times Vt \times T_2 \times ln(con1)) - (Tr \times Eg_{T1} - Eg_{T2}); \]
\[ Is_{T2} = \text{Area} \times Is \times \text{pow}(Tr, (Xti/N)) \times \text{limexp}(-('P_Q \times Eg_{T1}) \times (1 - Tr) / ('P_K \times T_2)); \]
\[ Cgs_{T2} = \text{Area} \times Cgs \times (1 + M \times (400e-6 \times (T_2 - T_1) - (Vbi_{T2} - Vbi) / Vbi)); \]
\[ Cgd_{T2} = \text{Area} \times Cgd \times (1 + M \times (400e-6 \times (T_2 - T_1) - (Vbi_{T2} - Vbi) / Vbi)); \]
\[ Vto_{T2} = Vto + Vtotc \times (T_2 - T_1); \]
\[ Gamma_{T2} = Gamma \times (1 + Gammatc \times (T_2 - T_1)); \]
\[ Alpha_{T2} = Alpha \times \text{pow}(1.01, Alphatc \times (T_2 - T_1)); \]

MESFET noise

Main components

- Thermal noise: generated by resistors Rg, Rd and Rs.
- Gate noise: Mainly channel noise induced in the gate (via the channel to gate capacitance) The resulting noise is amplified by the MESFET. The capacitive coupling causes the gate noise to have a power spectral density proportional to frequency.
- Flicker noise: Due to random carrier generation-recombination in the lattice imperfections or contaminating impurities. Flicker noise power has a \(1/f^n\) behavior, with \(n \approx 1\).

A typical plot of GaAs MESFET Ids noise current is shown in Fig. 19, where the
device drain to source noise current is given by

\[ I_{dsn} = \text{channel-thermal-noise-current} + \text{flicker-noise-current} \quad (47) \]

To a first approximation:

- **Channel-thermal-noise-current**
  \[ \text{Channel-thermal-noise-current}^7 = \sqrt{\frac{8 \cdot K \cdot T}{3} \cdot gm \cdot \left\{ \frac{1 + \alpha + \alpha^2}{1 + \alpha} \right\} \cdot G_{ds no i}} \]
  Where \( gm = \frac{\partial I_{ds}}{\partial V_{gs}} \),
  and \( \alpha = 1 - \frac{V_{ds}}{V_{gs} - V_{to}} \), when \( V_{ds} < \frac{3}{\text{Alpha}} \) – Linear region of operation
  Or \( \alpha = 0 \), when \( V_{ds} >= \frac{3}{\text{Alpha}} \) – Saturation region of operation

- **flicker-noise-current**
  \[ \text{flicker-noise-current} = \sqrt{K_f \cdot I_{ds}^{Af} \over f} \]

- Resister thermal noise equations
  \[ IR_{gn} = \sqrt{4 \cdot K \cdot T \over R_g}, \quad IR_{dn} = \sqrt{4 \cdot K \cdot T \over R_d}, \]
  and \[ IR_{sn} = \sqrt{4 \cdot K \cdot T \over R_s} \]
Figure 20: Typical GaAS MESFET equivalent circuit illustrating noise current components

MESFET equivalent circuit with noise current components

Curtice hyperbolic tangent model: LEVEL = 1 or 2: Noise equations

1. Verilog-A equations

fourkt=4.0*'P_K*T2;
gm=2*Beta_T2*(V(b1)-Vto_T2)*(1+Lambda*V(b3))*tanh(Alpha_T2*V(b3));
if ( V(b3) < 3/Alpha ) begin
    An=1-V(b3)/(V(b1)-Vto_T2);
    thermal_pwr= (8*'P_K*T2*gm/3)*((1+An+An*An)/(1+An))*Gdsnoi;
end else
    thermal_pwr=(8*'P_K*T2*gm/3)*Gdsnoi;
I(b3)<+white_noise(thermal_pwr,"thermal"); flicker_pwr = Kf*pow(Ids,Af);
I(b3)<+flicker_noise(flicker_pwr,1.0,"flicker");
end if
I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");
I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal");

---

Tsitvilds and Yanis, Operation and modeling of the MOS transistor, McGraw-Hill 1987, p340

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I(b9) <> white_noise(Area*fourkt/Rs_T2, "thermal");

2. Typical noise simulation results

Figure 21: Typical LEVEL 1 (or 2) GaAS MESFET Ids noise characteristic

Statz et. al. (Raytheon) model: LEVEL = 3: Noise equations

1. Verilog-A equations

if ( V(b3) < 3/Alpha ) begin
H1=(1-(1-(Alpha*V(b3))/3))/(1+B*(V(b1)-Vto_T2));

\[ gm=2*Beta_T2*(V(b1)-Vto_T2)*(1+Lambda*V(b3))*H1+(Beta_T2*(1+Lambda*V(b3))*pow((V(b1)-Vto_T2),2))*B*H1/(1+B*(V(b1)-Vto_T2)); \]

An=1-V(b3)/(V(b1)-Vto_T2);

\[ \text{thermal}_pwr= (8*P_K*T2*gm/3)*((1+An+An*An)/(1+An))\cdot Gdsnoi; \]

end 

else begin

\[ gm=2*Beta_T2*(V(b1)-Vto_T2)*(1+Lambda*V(b3))/(1+B*(V(b1)-Vto_T2)) + (Beta_T2*(1+Lambda*V(b3))*pow((V(b1)-Vto_T2),2))*B/pow(1+B*(V(b1)-Vto_T2),2); \]

\[ \text{thermal}_pwr=(8*P_K*T2*gm/3)*Gdsnoi; \]

end

I(b3) <+ white_noise(thermal\_pwr, "thermal");

\[ \text{flicker}_pwr = Kf* pow(Ids, Af); \]

I(b3) <+ flicker_noise(flicker\_pwr, 1.0, "flicker");

I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");

I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal");

I(b9) <+ white_noise(Area*fourkt/Rs_T2, "thermal");

2. Typical noise simulation results

**TriQuint Semiconductor TOM 1 model: LEVEL = 4: Noise equations**

1. Verilog-A equations

\[ \text{if ( V(b3) < 3/Alpha )begin} \]

\[ Ids1=(Beta_T2*\text{pow}( (V(b1)-Vto_T2), Qp ))*(1-\text{pow}( (1-Alpha*V(b3)/3), 3)); \]

\[ gm1=Qp*Beta_T2*\text{pow}( V(b1)-Vto_T2, Qp-1)\cdot(1-(1-\text{pow}(Alpha*V(b3)/3, 3))); \]

\[ gm=(gm1*(1+Lambda*V(b3))/(1+Delta*V(b1)*Ids1))*(1+(Delta*V(b3)*Ids1)/(1+Delta*V(b3)*Ids1)); \]

\[ An=1-V(b3)/(V(b1)-Vto_T2); \]

\[ \text{thermal}_pwr= (8*P_K*T2*gm/3)*((1+An+An*An)/(1+An))\cdot Gdsnoi; \]

end 

else begin

\[ Ids1=(Beta_T2*\text{pow}( (V(b1)-Vto_T2), Qp )); \]

\[ gm1=Qp*Beta_T2*\text{pow}( V(b1)-Vto_T2, Qp-1)); \]

\[ gm=(gm1*(1+Lambda*V(b3))/(1+Delta*V(b1)*Ids1))*(1+(Delta*V(b3)*Ids1)/(1+Delta*V(b3)*Ids1)); \]

\[ \text{thermal}_pwr=(8*P_K*T2*gm/3)*Gdsnoi; \]

end
Figure 22: Typical LEVEL 3 GaAS MESFET Ids noise characteristic

I(b3) <+ white_noise(thermal_pwr, "thermal");
flicker_pwr = Kf*pow(Ids, Af);
I(b3) <+ flicker_noise(flicker_pwr, 1.0, "flicker");
I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");
I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal");
I(b9) <+ white_noise(Area*fourkt/Rs_T2, "thermal");

2. Typical noise simulation results

TriQuint Semiconductor TOM 2 model: LEVEL = 5

1. Verilog-A equations

if ( V(b3) < 3/Alpha ) begin
   Nst=Ng+Nd*V(b3);
   if ( Nst < 1.0) Nst=1.0;
   Vst=Nst*Vt_T2;
   Vg=Qp*Vst*ln( exp( (V(b1)-Vto_T2+Gamma_T2*V(b3)) / (Qp*Vst) ) + 1);
Figure 23: Typical LEVEL 4 GaAS MESFET Ids noise characteristic

\[
A_1 = \text{Alpha}_T \cdot \text{V}(b3); \quad F_d = A_1 / \sqrt{1 + (A_1 \cdot A_1)};
\]

\[
I_{ds1} = \text{Beta}_T \cdot \text{pow}(V_g, Qp) \cdot F_d;
\]

\[
g_m_1 = \frac{I_{ds1}}{V_g} \cdot Qp / \left( \exp\left(-\frac{(V(b1) - V_{to} + \Delta \cdot V(b3))}{Qp \cdot Vst}\right) + 1 \right);
\]

\[
g_m = \frac{g_m_1}{\left(1 + \Delta \cdot V(b3) \cdot I_{ds1}\right)^2};
\]

\[
\text{thermal}_\text{pwr} = (8 \cdot P_K \cdot T_2 \cdot g_m / 3) \cdot \left(1 + An + An \cdot An / (1 + An)\right) \cdot Gdsnoi;
\]

```
end
else begin

Nst = Ng + Nd \cdot \text{V}(b3); if (Nst < 1.0) Nst = 1.0;
Vst = Nst \cdot Vt_T2;
Vg = Qp \cdot Vst \cdot \ln\left(\exp\left(\frac{(V(b1) - V_{to} + \Gamma_T \cdot V(b3))}{Qp \cdot Vst}\right) + 1\right);

A_1 = \text{Alpha}_T \cdot \text{V}(b3); \quad F_d = A_1 / \sqrt{1 + (A_1 \cdot A_1)};
I_{ds1} = \text{Beta}_T \cdot \text{pow}(V_g, Qp) \cdot F_d;

\[
g_m_1 = \frac{I_{ds1}}{V_g} \cdot Qp / \left( \exp\left(-\frac{(V(b1) - V_{to} + \Delta \cdot V(b3))}{Qp \cdot Vst}\right) + 1 \right);
\]

\[
g_m = \frac{g_m_1}{\left(1 + \Delta \cdot V(b3) \cdot I_{ds1}\right)^2};
\]

\[
\text{thermal}_\text{pwr} = (8 \cdot P_K \cdot T_2 \cdot g_m / 3) \cdot Gdsnoi;
\]

end
```

I(b3) <+ white_noise(thermal_pwr, "thermal");

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flicker_pwr = Kf*pow(Ids,Af);
I(b3) <+ flicker_noise(flicker_pwr,1.0, "flicker");
I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");
I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal");
I(b9) <+ white_noise(Area*fourkt/Rs_T2, "thermal");

2. Typical noise simulation results

![Figure 24: Typical LEVEL 5 GaAS MESFET Ids noise characteristic](image)

**Adding external passive components to the MESFET models**

The Curtice model outlined in the first Qucs report on MESFETs included lead inductance in each of the device signal paths. These inductances were not included in the Verilog-A models described in this report, mainly to simplify the model code. If required they can be added as external components. The test circuit shown in Fig. 25 indicates how this can be done and illustrates the effect such components have on the Curtice S parameter characteristics.
Figure 25: S parameter simulated characteristics for test circuit shown in Fig. 5 that has external inductance added
MESFETs are important high frequency devices which have been missing from the range of active component models supplied with Qucs. While developing the models described in this report I have attempted to make them as flexible as possible so as to allow users the opportunity to select which model, or indeed the make-up of the components of a model, they would like to try for a specific simulation. The work described in this report is very much work in progress, mainly because there are a number of other published MESFET models that have not been included. My intention has simply been to provide a number of practical models which were not previously available to Qucs users. Also knowing that many Qucs users have an interest in high frequency circuit design and simulation, the work would be of direct relevance to making Qucs more “universal”. The procedures employed for model development are another example of the work being undertaken by the Qucs team in response to Qucs being adopted by the wider modelling community as part of the Verilog-A compact device standardization project. Overall the simulation results from the models described here show a high degree of consistency from DC to the high frequency S parameter domain. The noise results are particularly interesting as they are based on mix of available theories and extensions introduced especially for Qucs. Some readers will probably have spotted one area where there appears to be differences in the simulation results from the different models; look at the S[1,2] and S[2,1] characteristics for each model. Here there are noticeable difference which are possibly due to the lack of symmetry in some of the model charge equations? MESFET modelling is a complex subject, suggesting that there are likely to be errors /bugs in the models. If you find an error/bug please inform the Qucs development team so that we can correct problems as they are found. In the future, particularly if the response to this group of models is positive, I will attempt to add more MESFET models to Qucs. Once again a special thanks to Stefan Jahn for all his help and encouragement over the period that I have been developing the Qucs MESFET models and writing the report which outlines their physical and mathematical fundamentals.