Qucs

A Report

Verilog-A compact device models for GaAs MESFETs

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Introduction

A previous Qucs Report[1] described a MESFET model based on an equation defined device (EDD) representation of the level 1 Curtice model. This model evolved as a test example during the initial Qucs EDD development phase. Today the EDD model is popular amongst Qucs users as either a powerful non-linear component in it's own right or as the basis of a component prototyping system for constructing compact Verilog-A device models, translated with ADMS to C++ code, compiled to object code and finally linked to the main body of the Qucs program code. Over the last year the Qucs development team has invested a significant amount of time improving both EDD prototyping and Verilog-A compact device/circuit model development, making the development process more transparent to anyone interested in trying their hand at model construction. One branch of the current Qucs modelling activities is concentrating on adding new models which fill in some of the gaps in the Qucs released model lists. One such model in this category is the GaAs MESFET. This report outlines the background and mathematical basis for a number of MESFET models. These have been coded in Verilog-A and tested using recent Qucs CVS code. They will be included in the next full release of Qucs.

The GaAs MESFET

The metal-semiconductor FET (MESFET) is a Schottky-barrier gate FET which is normally made from Gallium Arsenide. It is a popular device for high frequency applications because of it's high electron mobility and usable gain at microwave frequencies. An early simulation model for the MESFET device was developed by Walter R. Curtice[2] in 1980 at the RCA Laboratory in Princeton, New Jersey, USA. Since Curtice published his original MEFET model a number of authors have contributed improvements to the basic model, including for example Statz *et. al.* (Raytheon)[3] and TriQuint Semiconductor Inc.[4]. These models form the basis of the Qucs MESFET model described in this report.

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[1] M. Brinson and S. Jahn, Qucs: Compact device- circuit macromodel specification; A Curtice level 1 MESFET model, http://qucs.sourceforge.net/docs.html

[2] W.R. Curtice, 1980, A MESFET model for use in the design of GaAs integrated circuits, IEEE Transactions on Microwave Theory and Techniques, MTT-28, pp. 448-456.

[3] H. Statz, P. Newman, I.W. Smith, R.A. Pucel, and H.A. Haus, gaAs FET Device and Circuit Simulation in SPICE, IEEE Transactions on Electron Devices, Vol. 34, pp. 160-169, Feb. 1987.

[4] For example, D.H. Smith, TOM-2: An improved Model for GaAs MESFETs, TriQuint Report, TriQuint Semiconductor, Inc Fe. 27, 1995 (11 pages).

The Qucs MESFET model

Parameters

Name	Symbol	Description	Unit	Default
LEVEL		model selector		1
Vto	V_{to}	gate threshold voltage	V	-1.8
Beta	β	transconductance parameter	A/V^2	3m
Alpha	α	coefficient of Vds in tanh function	1/V	2.25
Gamma	γ	dc drain pull coefficient		0.015
Lambda	λ	channel length modulation parameter	1/V	0.05
B	B	doping profile parameter	1/V	0
Qp	Qp	power law exponent parameter		2.1
Delta	δ	power feedback parameter	1/W	0.1
Vmax	$Vmax$	maximum junction voltage before cap. limiting	V	0.5
Vdelta1	$Vdelta1$	capacitance saturation transition voltage	V	0.3
Vdelta2	$Vdelta2$	capacitance threshold transition voltage	V	0.2
Nsc	Nsc	subthreshold conductance parameter		1
Is	I_S	diode saturation current	A	10f
N	N	diode emission coefficient		1
Vbi	Vbi	built-in gate potential	V	1.0
Bv	Bv	diode breakdown voltage	V	60
XTI	X_{TI}	diode saturation current temperature coefficient		0
TAU	τ	internal time delay from drain to source	s	10p
Rin	Rin	series resistance to Cgs	Ω	1m
Fc	Fc	forward-bias depletion capacitance coefficient		0.5
Area	$Area$	area factor		1
Eg	Eg	bandgap voltage	V	1.11
M	M	grading coefficient		0.5
Cgs	Cgs	zero-bias gate-source capacitance	F	0.2p
Cgd	Cgd	zero-bias gate-drain capacitance	F	1p
Cds	Cds	zero-bias drain-source capacitance	F	1p
Betatc	$Betatc$	Beta temperature coefficient	%/C	0
Alphatc	$Alphatc$	Alpha temperature coefficient	%/C	0
Gammatc	$Gammatc$	Gamma temperature coefficient	%/C	0
Ng	Ng	subthreshold slope gate parameter		2.65
Nd	Nd	subthreshold drain pull parameter		-0.19

Name	Symbol	Description	Unit	Default
ILEVELS	$ILEVELS$	gate-source current equation selector		3
ILEVELD	$ILEVELD$	drain-source current equation selector		3
QLEVELS	$QLEVELS$	gate-source charge equation selector		2
QLEVELD	$QLEVELS$	gate-source charge equation selector		2
QLEVELDS	$QLEVELDS$	drain-source charge equation selector		2
Vtotc	$Vtotc$	Vto temperature coefficient	V/C	0
Rg	Rg	gate series resistance	Ω	5.1
Rd	Rd	drain series resistance	Ω	1.3
Rs	Rs	source series resistance	Ω	1.3
Rgtc	$Rgtc$	gate series resistance temperature coefficient	1/C	0
Rdtc	$Rdtc$	drain series resistance temperature coefficient	1/C	0
Rstc	$Rstc$	source series resistance temperature coefficient	1/C	0
Ibv	Ibv	gate reverse breakdown current	A	1m
Rf	Rf	forward bias slope resistance	Ω	10
R1	$R1$	breakdown slope resistance	Ω	10
Af	Af	Flicker noise exponent		1.0
Kf	Kf	flicker noise coefficient		0.0
Gdsnoi	$Gdnsnoi$	shot noise coefficient		1.0
Tnom	$Tnom$	device parameter measurement temperature	°C	26.85
Temp	$Temp$	device circuit temperature	°C	26.85

Where parameter LEVEL selects a MESFET model listed in Table 2.

LEVEL	MESFET model type
1	Quadratic Curtice - basic form
2	Quadratic Curtice - basic plus subthreshold properties
3	Statz et. al. (Raytheon) - same as SPICE 3f5
4	TriQuint - TOM 1 model
5	TriQuint - TOM 2 model

Table 2: Qucs MESFET model types

MESFET gate current equations can be selected by setting parameters ILEVELS and ILEVELD. Table 3 lists the available options.

MESFET charge equations can be selected by setting parameters QLEVELS, QLEVELD and QLEVELDS. Table 4 lists the available options. Although it

ILEVELS - ILEVELD	Gate-source current	Gate-drain current
0	Igs=0	Igd=0
1	Linear no reverse breakdown	Linear no reverse breakdown
2	Linear with reverse breakdown	Linear with reverse breakdown
3	Diode no reverse breakdown	Diode no reverse breakdown
4	Diode with reverse breakdown	Diode with reverse breakdown

Table 3: Qucs MESFET gate current model types

is possible to mix the five basic MESFET models with different gate current and charge equation models the common default models are the ones listed in Table 5.

QLEVELS		QLEVELD		QLEVELDS	
0	Qgs=0	0	Qgd=0	0	Qds=0
1	Constant cap.	1	Constant cap.	1	Constant cap.
2	Diode	2	Diode	2	Constant cap.+ transit
3	Statz	3	Statz		

Table 4: Qucs MESFET charge equation types

Model	LEVEL	ILEVELS	ILEVELD	QLEVELS	QLEVELD	QLEVELDS
Curtice L1	1	0 to 4	0 to 4	0 to 2	0 to 2	0 to 2
Curtice (Adv.)	2	0 to 4	0 to 4	0 to 2	0 to 2	0 to 2
Statz-Raytheon	3	4	4	3	3	2
TOM 1	4	4	4	3	3	2
TOM 2	5	4	4	3	3	2

Table 5: Qucs MESET default selection parameters

The Qucs MESFET simulation model

The large signal equivalent circuit for the Qucs MESFET model is illustrated in Fig. 1. The currents flowing in each of the circuit branches are given by the Verilog-A code fragment shown in Fig. 1. The Verilog-A HDL code for the entire Qucs MESFET model is available from the Qucs CVS archive[5]. In order to simulate

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[5] http://qucs.sourceforge.net/

the operation of an MESFET, equations based on the physical operation of the device are required for all the current contribution components in Fig. 1. These equations are presented in the remaining sections of this report. Examples are also introduced to demonstrate the simulation performance of each model.

MESFET gate current equations

- ILEVELS = 0: $Igs = 0$ A
- ILEVELS = 1: if $(V(b1) > Vbi)$

$$Igs = \frac{V(b1) - Vbi}{Rf} \tag{1}$$

else $$Igs = -Area \cdot Is + GMIN \cdot V(b1)$$

- ILEVELS = 2: if $(V(b1) > Vbi)$

$$Igs1 = \frac{V(b1) - Vbi}{Rf} \tag{2}$$

else $$Igs1 = -Area \cdot Is + GMIN \cdot V(b1)$$

if $V(b1) < -Bv)$

$$Igs2 = \frac{V(b1) - Vbi}{R1} \tag{3}$$

$$Igs = Igs1 + Igs2 \tag{4}$$

- ILEVELS = 3: if $(V(b1) > Vbi)$

$$Igs = Is\_T2 \cdot \left\{ limexp\left(\frac{V(b1)}{N \cdot Vt\_T2}\right) - 1.0 \right\} + GMIN \cdot V(b1) \tag{5}$$

else $Igs = -Is\_T2 + GMIN \cdot V(b1)$

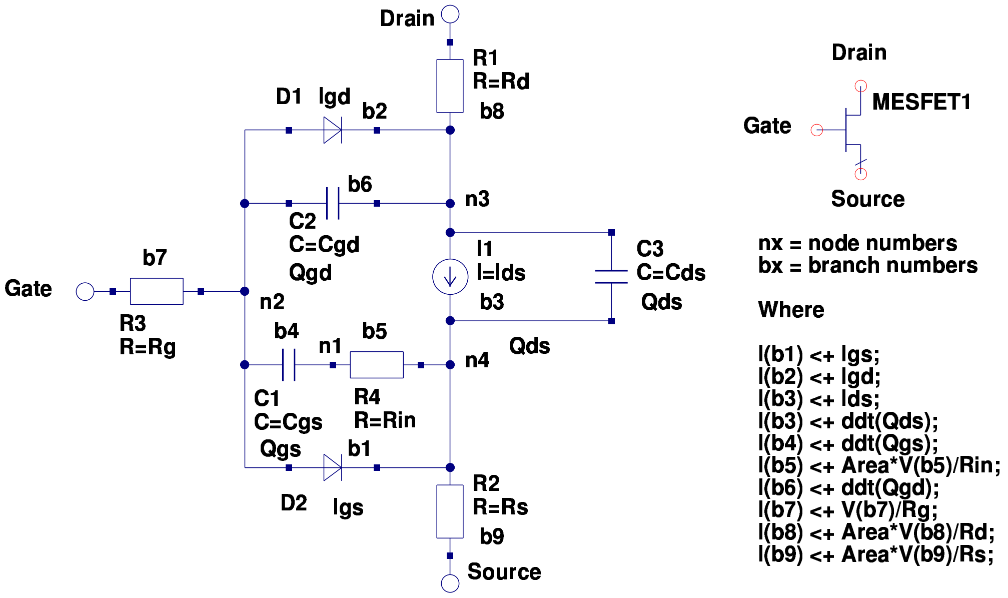
- ILEVELS = 4: if $(V(b1) > -5 \cdot N \cdot Vt\_T2)$

$$Igs1 = Area \cdot Is\_T2 \cdot \left\{ limexp\left(\frac{V(b1)}{N \cdot Vt\_T2}\right) - 1.0 \right\} + GMIN \cdot V(b1) \tag{6}$$

else $Igs1 = 0$

if $((-Bv < V(b1))$ and $(V(b1) < -5 \cdot N \cdot Vt\_T2))$

$$Igs2 = -Area \cdot Is\_T2 + GMIN \cdot V(b1) \tag{7}$$



```
I(b1) <+ Igs;
I(b2) <+ Igd;
I(b3) <+ Ids;
I(b3) <+ ddt(Qds);
I(b4) <+ ddt(Qgs);
I(b5) <+ Area*V(b5)/Rin;
I(b6) <+ ddt(Qgd);
I(b7) <+ V(b7)/Rg;
I(b8) <+ Area*V(b8)/Rd;
I(b9) <+ Area*V(b9)/Rs;
```

Figure 1: Qucs MESFET symbol and large signal equivalent circuit

else $\quad Igs2 = 0$

if $(V(b1) == -Bv)$

$$Igs3 = -Ibv \tag{8}$$

else $\quad Igs3 = 0$

if $(V(b1) < -Bv)$

$$Igs4 = -Area \cdot Is\_T2 \cdot \left\{ limexp\left(\frac{-(Bv + V(b1))}{Vt\_T2} \right) - 1.0 + \frac{Bv}{Vt\_T2} \right\} \tag{9}$$

else $\quad Igs4 = 0$

$$Igs = Igs1 + Igs2 + Igs3 + Igs4 \tag{10}$$

Where xx_T2 indicates the values of temperature dependent parameters at circuit temperature T2. See later sections of this report for more details. The gate to drain current equations are identical except Igs is replaced by Igd, Igsx by Igdx, and V(b1) by V(b2). More details can be found in the Verilog-A listing given in the Qucs CVS code held at the Qucs Sourceforge site.

MESFET charge equations QLEVELS 0 to 2

- QLEVELS = 0: [NO charge]:

$$Qgs = 0 \tag{11}$$

- QLEVELS = 1: [Fixed capacitor charge]

$$Qgs = Area \cdot Cgs \cdot V(b4) \tag{12}$$

- QLEVELS = 2: [Diode charge]
  if $(V(b4) < (Fc \cdot Vbi))$

$$Qgs1 = \frac{Cgs\_T2 \cdot Vbi\_T2}{(1-M)} \cdot \left\{1 - \left(1 - \frac{V(b4)}{Vbi\_T2}\right)^{1-M}\right\} \tag{13}$$

if $(V(b4) >= (Fc \cdot Vbi))$

$$H1 = \frac{M}{2 \cdot Vbi\_T2} \cdot \left(V(b4) \cdot V(b4) - (Fc \cdot Fc \cdot Vbi\_T2 \cdot Vbi\_T2)\right) \tag{14}$$

$$Qgs2 = Cgs\_T2 \cdot \left[F1 + \frac{1}{F2} \cdot \{F3 \cdot \left(V(b4) - Fc \cdot Vbi\_T2\right) + H1\}\right] \tag{15}$$

Where,

$$F1 = \frac{Vbi\_T2}{1-M} \cdot \left\{1 - (1-Fc)^{1-M}\right\}, \tag{16}$$

$$F2 = (1-Fc)^{1+M}, \tag{17}$$

and

$$F3 = 1 - Fc \cdot \left(1+M\right). \tag{18}$$

Again xx_T2 indicates the values of temperature dependent parameters at circuit temperature T2. See a later section of this report for more details. The gate to drain charge equations (types 0 to 2) are identical except Qgs is replaced by Qgd, Qgsx by Qgdx, and V(b4) by V(b6). More details can be found in the Qucs CVS code held at the Qucs Sourceforge site.

MESFET charge equations QLEVELDS 0 to 2

- QLEVELDS = 0: [NO charge]:

$$Qds = 0 \tag{19}$$

- QLEVELDS = 1: [Fixed capacitor charge]

$$Qds = Area \cdot Cds \cdot V(b3) \tag{20}$$

- QLEVELS = 2: [Fixed capacitor plus transit charge]

$$Qds = Area \cdot Cds \cdot V(b3) + Tau \cdot Ids \tag{21}$$

Curtice hyperbolic tangent model: LEVEL = 1

if $(V(b1) - Vto\_T2) > 0$

$$Ids = Beta\_T2 \cdot (V(b1) - Vto\_T2)^2 \cdot \{1 + Lambda \cdot V(b3)\} \cdot tanh(Alpha \cdot V(b3)) \tag{22}$$

else $Ids = 0$.

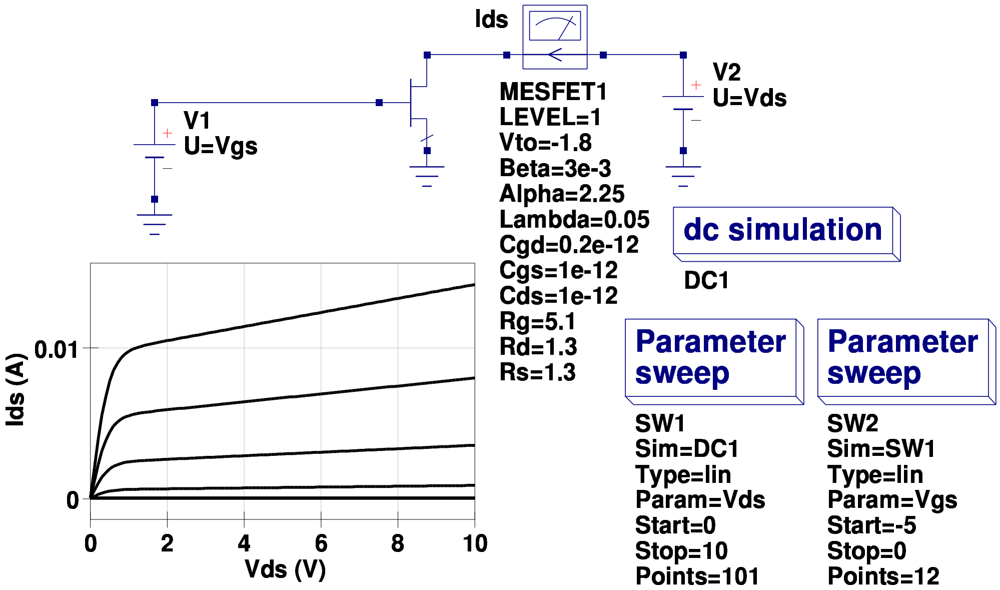


Figure 2: Curtice LEVEL 1 DC test circuit and Ids-Vds characteristics

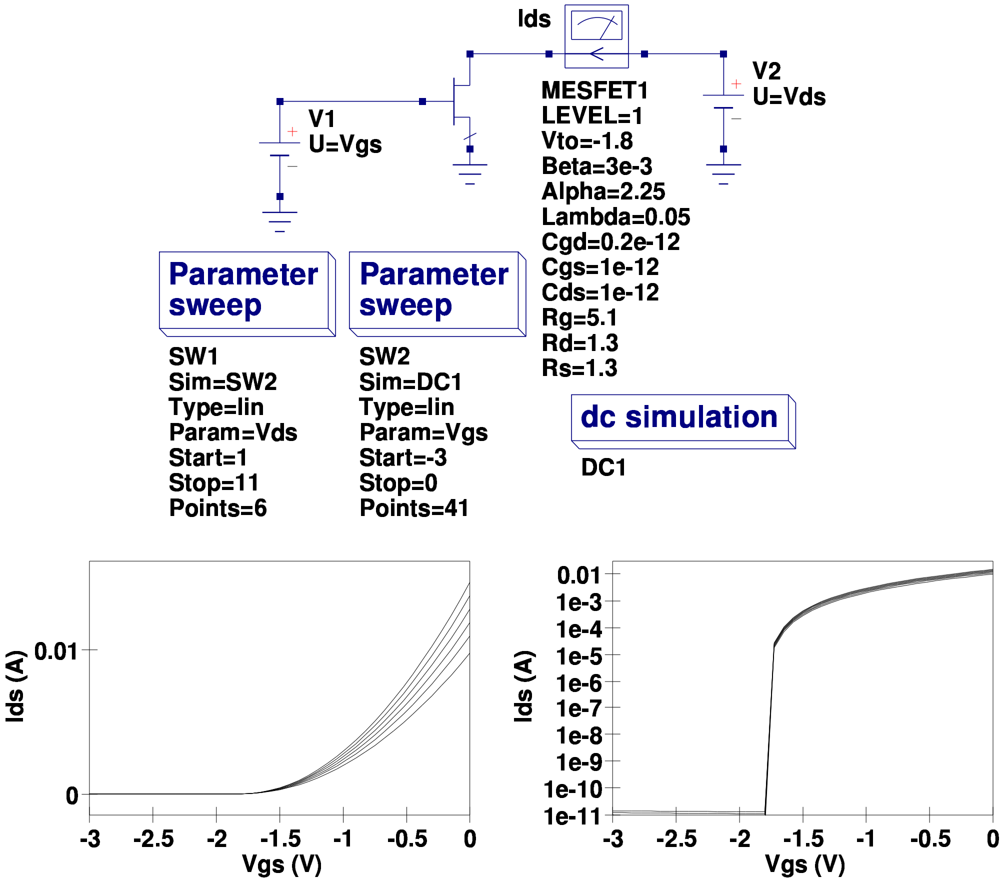


Figure 3: Curtice LEVEL 1 DC test circuit and Ids-Vgs characteristics

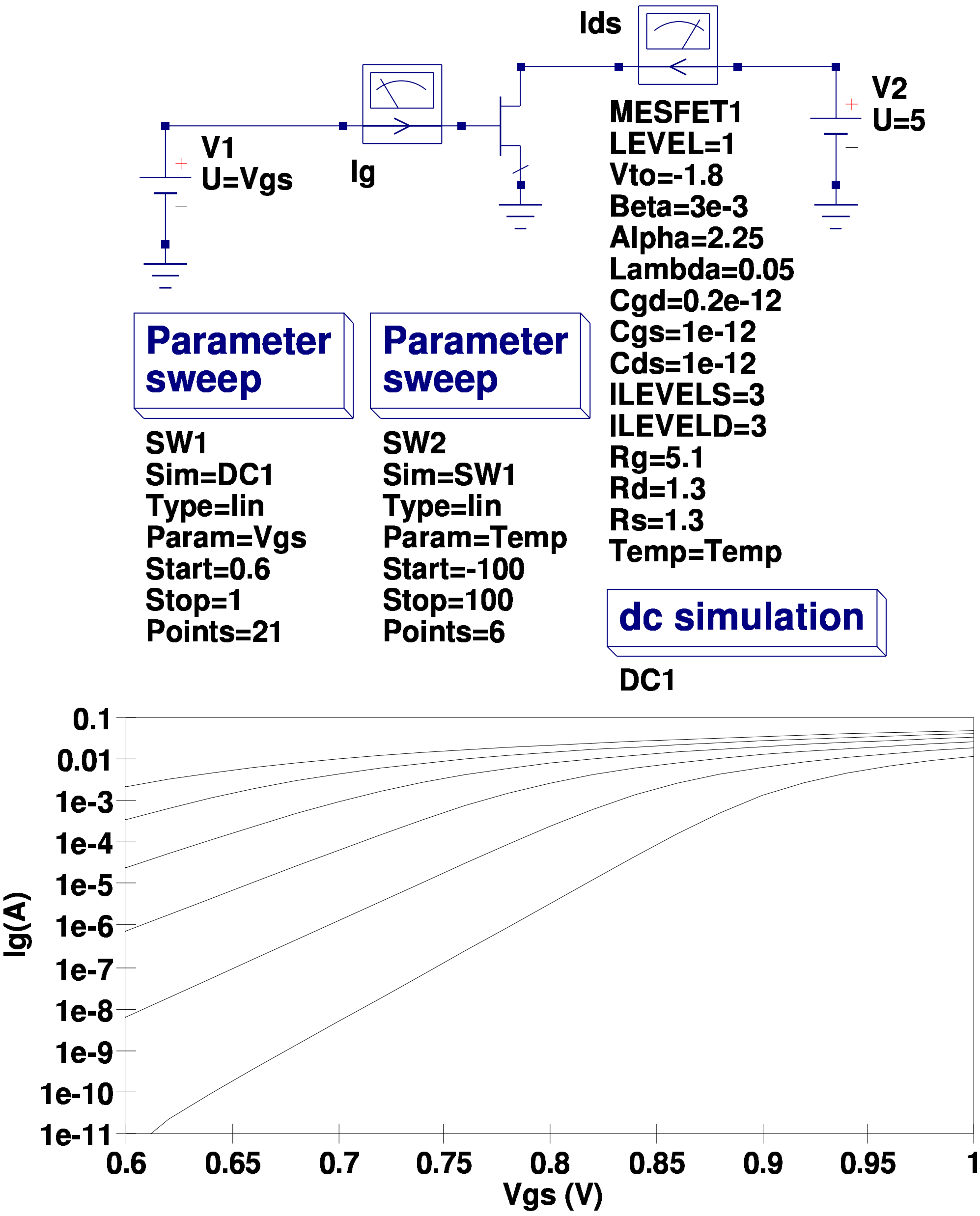


Figure 4: Curtice LEVEL 1 DC test circuit and Ig-Vgs characteristics

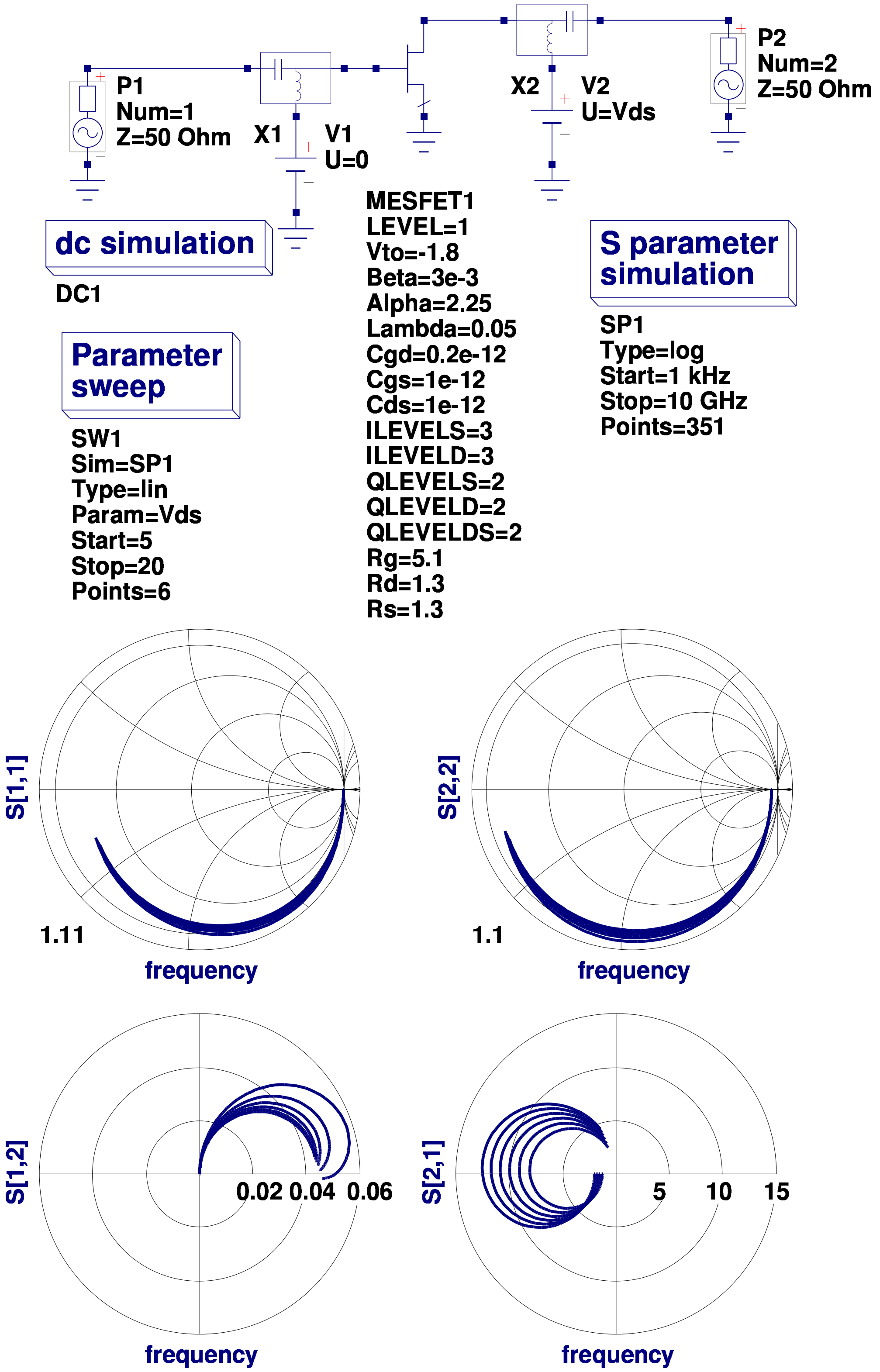


Figure 5: Curtice LEVEL 1 S parameter test circuit and characteristics

Curtice hyperbolic tangent model with subthreshold modification: LEVEL = 2

$$Ids = Beta\_T2 \cdot Vf^2 \cdot \{1 + Lambda \cdot V(b3)\} \cdot tanh(Alpha \cdot V(b3)) \tag{23}$$

Where

$$Vf = \frac{1}{Ah} \cdot ln\left\{1 + exp\left(Ah \cdot (V(b1) - Vto\_T2)\right)\right\} \tag{24}$$

and

$$Ah = \frac{1}{2 \cdot Nsc \cdot Vt\_T2} \tag{25}$$

When $V(b2) > Vto\_T2, Vf \Longrightarrow V(b2) - Vto\_T2$. Otherwise, Vf approaches zero asymptotically. This modification to the basic Curtice model provides an improved match to channel gradual pinch-off and MESFET subthreshold conduction.

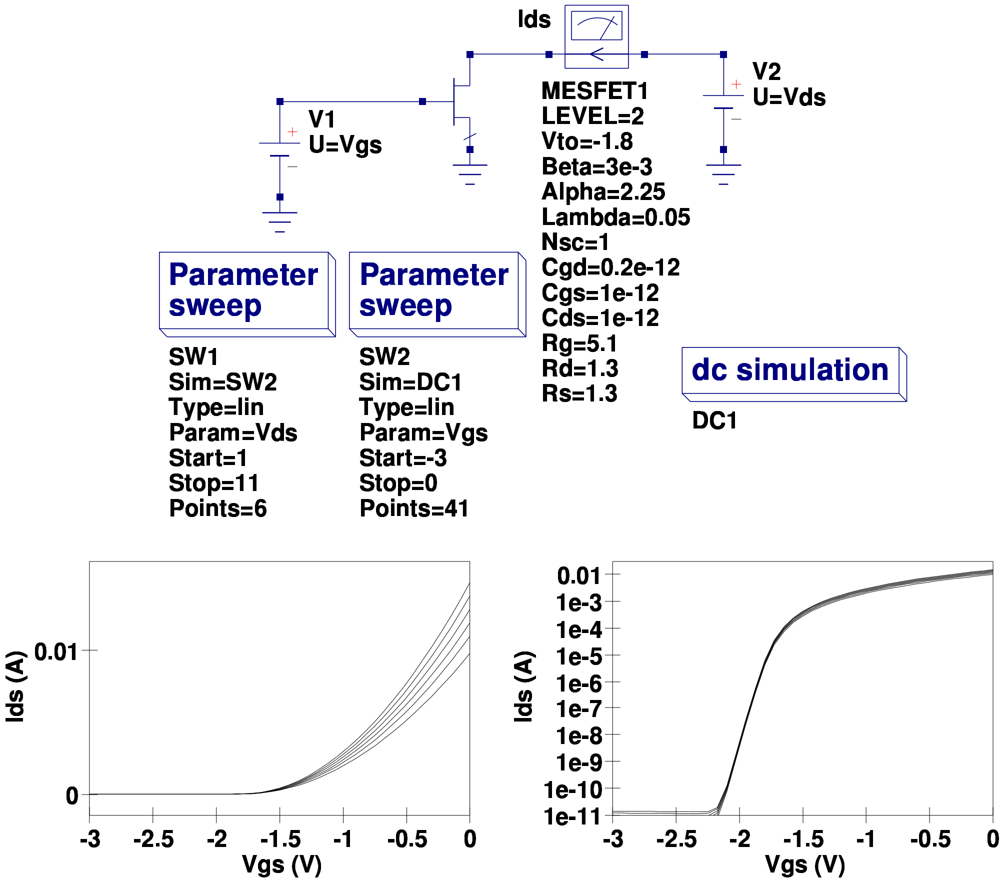


Figure 6: Curtice LEVEL 2 DC test circuit and Ids-Vgs characteristics illustrating subthreshold conduction modification

Statz *et. al.* (Raytheon) model: LEVEL = 3

if $(V(b1) - Vto\_T2) > 0$

if $(0 < V(b3))$ and $(V(b3) < \frac{3}{Alpha})$

begin

$$H1 = \frac{1 - \left\{1 - \frac{Alpha \cdot V(b3)}{3}\right\}^3}{1 + B \cdot (V(b1) - Vto\_T2)} \tag{26}$$

$$Ids = Beta\_T2 \cdot \{1 + Lambda \cdot V(b3)\} \cdot (V(b1) - Vto\_T2)^2 \cdot H1 \tag{27}$$

end

if $(V(b3) > \frac{3}{Alpha})$

$$Ids = \frac{Beta\_T2 \cdot \{1 + Lambda \cdot V(b3)\} \cdot (V(b1) - Vto\_T2)^2}{1 + B \cdot (V(b1) - Vto\_T2)} \tag{28}$$

else $Ids = 0$.

MESFET charge equations QLEVELS = 3 and QLEVELD = 3

QLEVELS = 3 : Statz et. al. charge equations

$$Vmax = min(Fc \cdot Vbi, Vmax) \tag{29}$$

$$Veff1 = 0.5 \cdot \left\{V(b4) + V(b6) + \sqrt{(V(b6) - V(b4))^2 + Vdelta1^2}\right\} \tag{30}$$

$$Vnew = 0.5 \cdot \left\{Veff1 + Vto\_T2 + \sqrt{(Veff1 - Vto\_T2)^2 + Vdelta2^2}\right\} \tag{31}$$

if $(Vnew > Vmax)$

$$Qgs = Cgs\_T2 \cdot \left\{2 \cdot Vbi\_T2 \left(1 - \sqrt{1 - \frac{Vmax}{Vbi\_T2}}\right) + \frac{Vnew - Vmax}{\sqrt{1 - \frac{Vmax}{Vbi\_T2}}}\right\} \tag{32}$$

if $(Vnew <= Vmax)$

$$Qgs = Cgs\_T2 \cdot 2 \cdot Vbi\_T2 \cdot \left\{1 - \sqrt{1 - \frac{Vnew}{Vbi\_T2}}\right\} \tag{33}$$

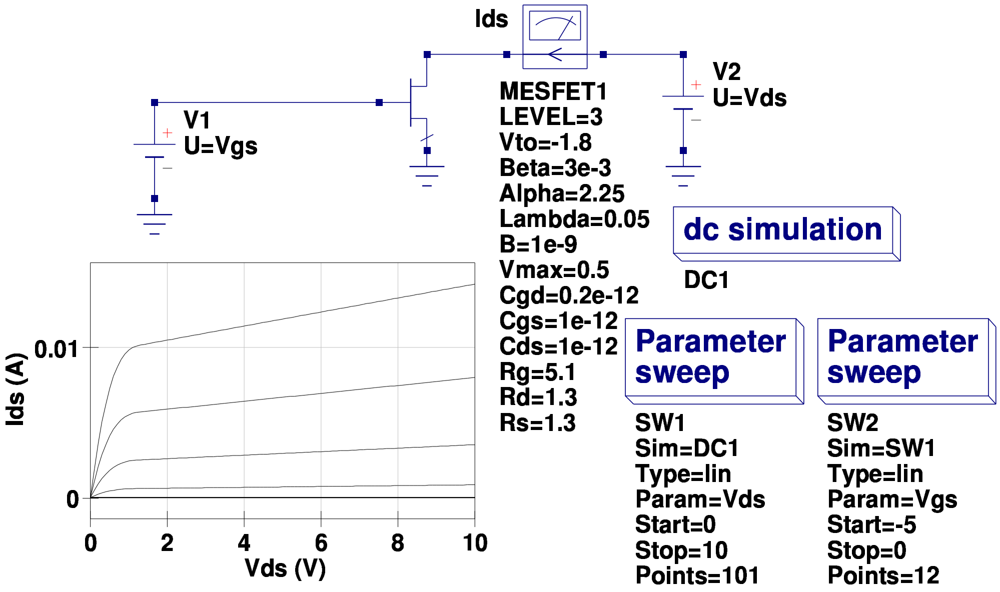


Figure 7: Statz *et. al.* LEVEL 3 DC test circuit and Ids-Vds characteristics

QLEVELD = 3 : Statz et. al. charge equations

$$Veff2 = 0.5 \cdot \left\{ V(b4) + V(b6) - \sqrt{(V(b4) - V(b6))^2 + Vdelta1^2} \right\} \tag{34}$$

$$Qds = Cgd\_T2 \cdot Veff2 \tag{35}$$

During simulation gate charge must be partitioned between gate-source and gate-drain branches. The Qucs implementation of the Statz et. al. MESFET model uses the procedure adopted by Divehar [6].

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[6] D. Divehar, Comments on GaAs FET device and circuit simulation in SPICE,IEEE Transactions on Electronic Devices, Vol. ED-34, pp 2564-2565, Dec. 1987

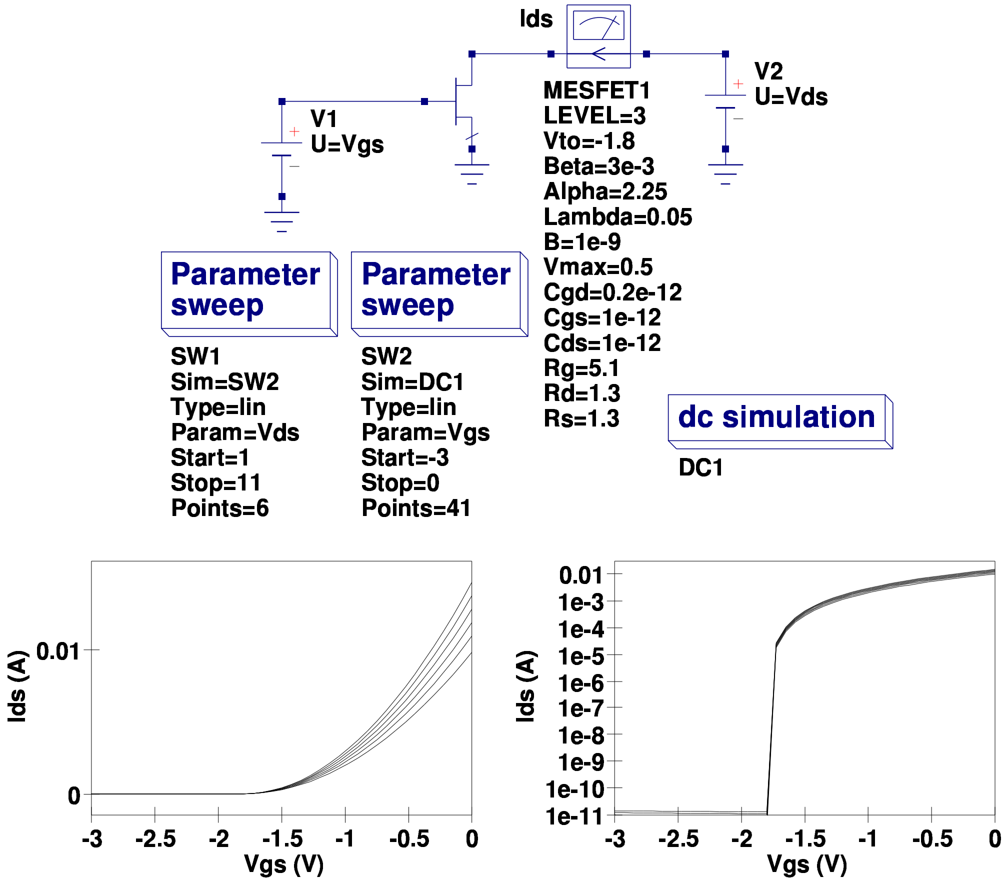


Figure 8: Statz *et. al.* LEVEL 3 DC test circuit and Ids-Vgs characteristics

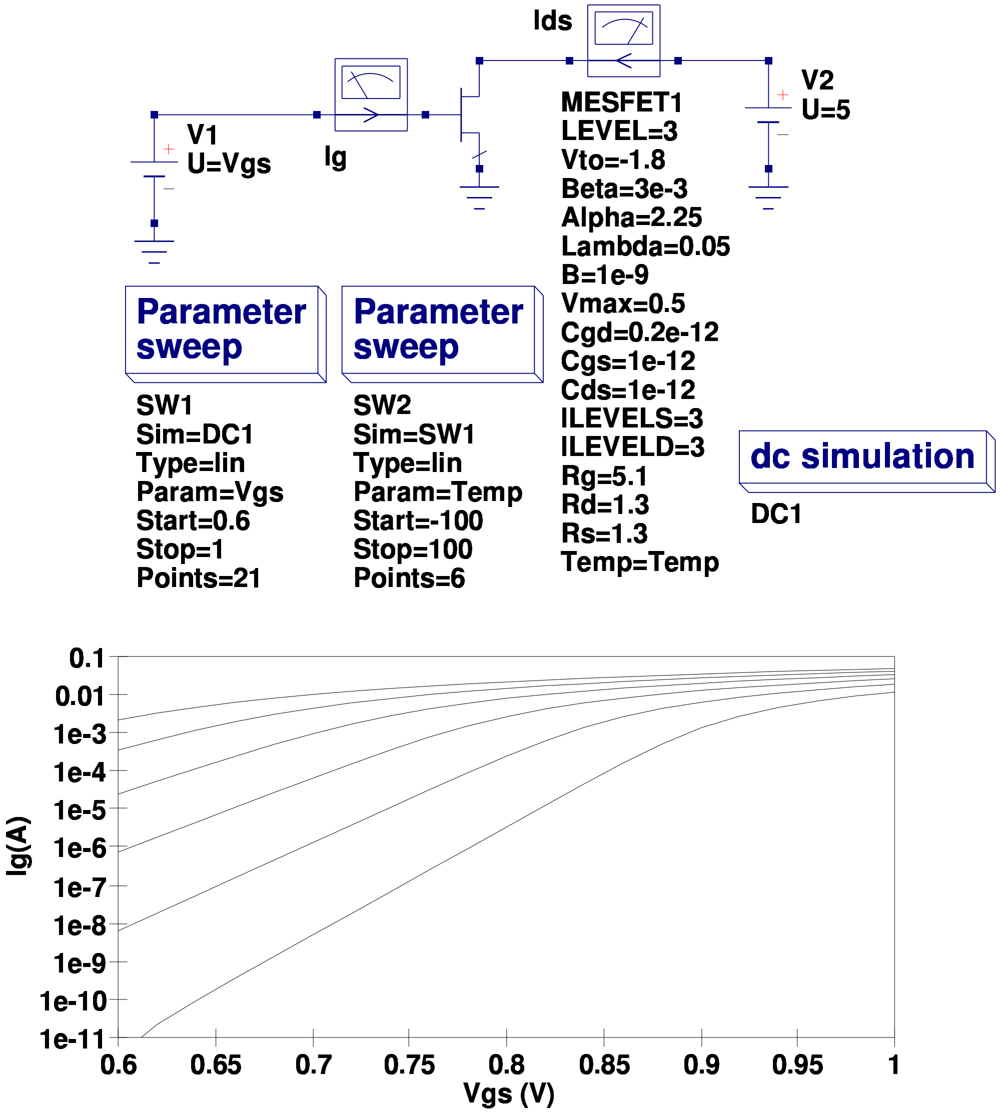


Figure 9: Statz *et. al.* LEVEL 3 DC test circuit and Ig-Vgs characteristics

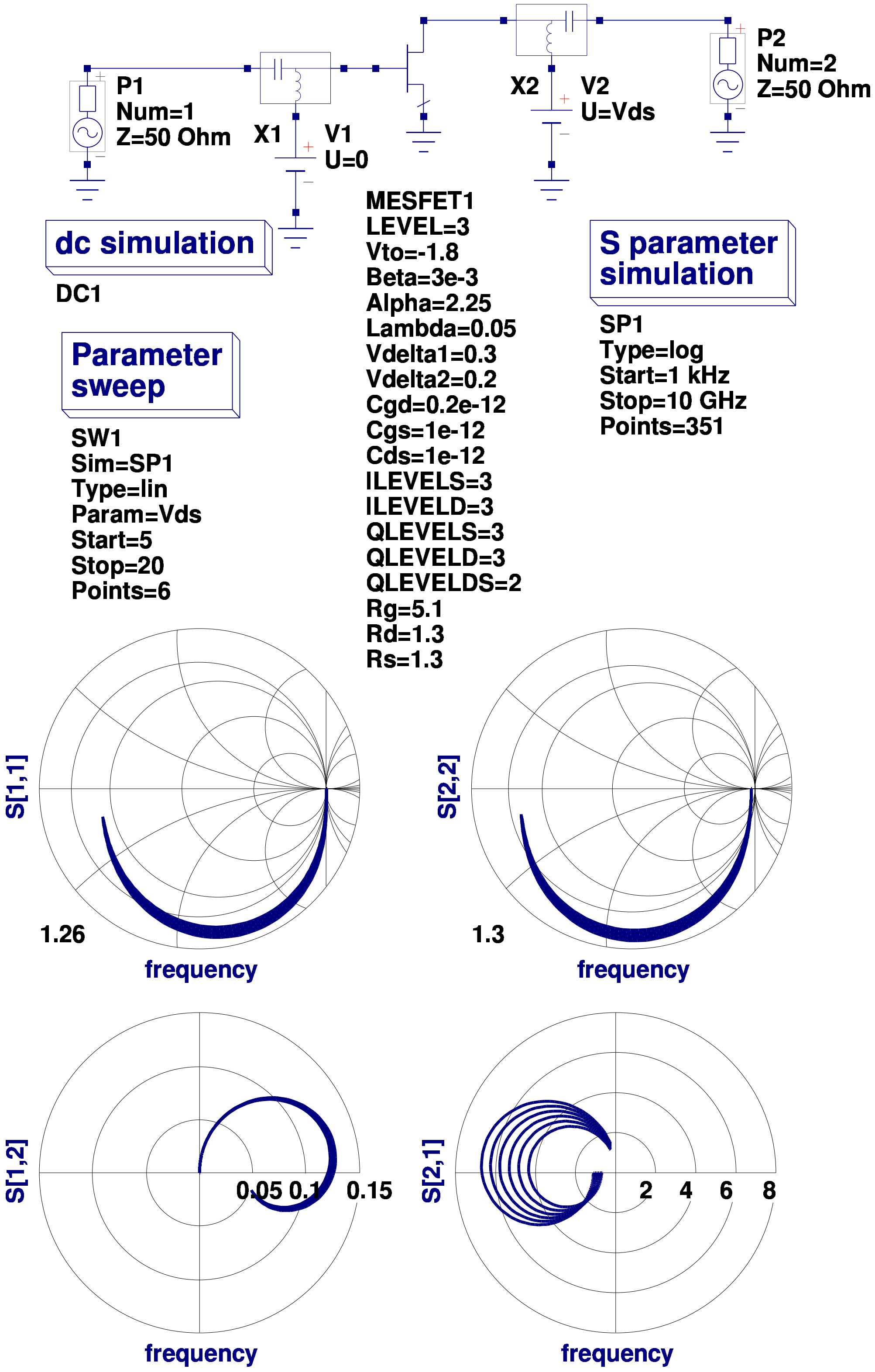


Figure 10: Statz *et. al.* LEVEL 3 S parameter test circuit and characteristics

TriQuint Semiconductor TOM 1 model: LEVEL = 4

if $(V(b1) - Vto\_T2) > 0$

if $(0 < V(b3))$ and $(V(b3) < \frac{3}{Alpha})$

begin

$$Ids1 = \left\{ Beta\_T2 \cdot (V(b1) - Vto\_T2)^{Qp} \right\} \cdot \left\{ 1 - \left\{ 1 - \frac{Alpha \cdot V(b3)}{3} \right\}^3 \right\} \tag{36}$$

$$Ids = \frac{Ids1 \cdot \{1 + Lambda \cdot V(b3)\}}{1 + Delta \cdot V(b3) \cdot Ids1} \tag{37}$$

end

if $(V(b3) > \frac{3}{Alpha})$

$$Ids1 = Beta\_T2 \cdot (V(b1) - Vto\_T2)^{Qp} \tag{38}$$

$$Ids = \frac{Ids1 \cdot \{1 + Lambda \cdot V(b3)\}}{1 + Delta \cdot (V(b3) \cdot Ids1} \tag{39}$$

else $Ids = 0$.

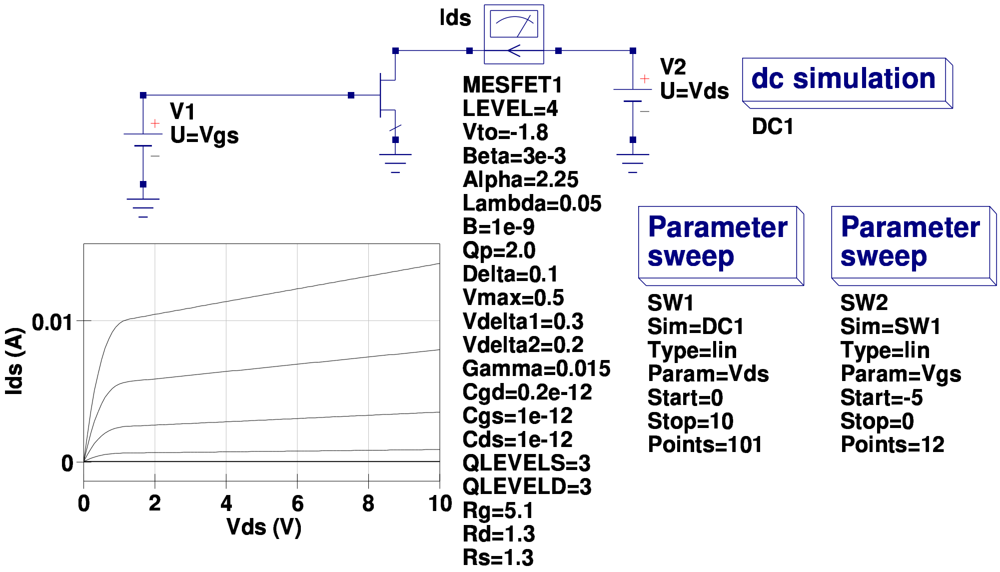


Figure 11: TOM1 LEVEL 4 DC test circuit and Ids-Vds characteristics

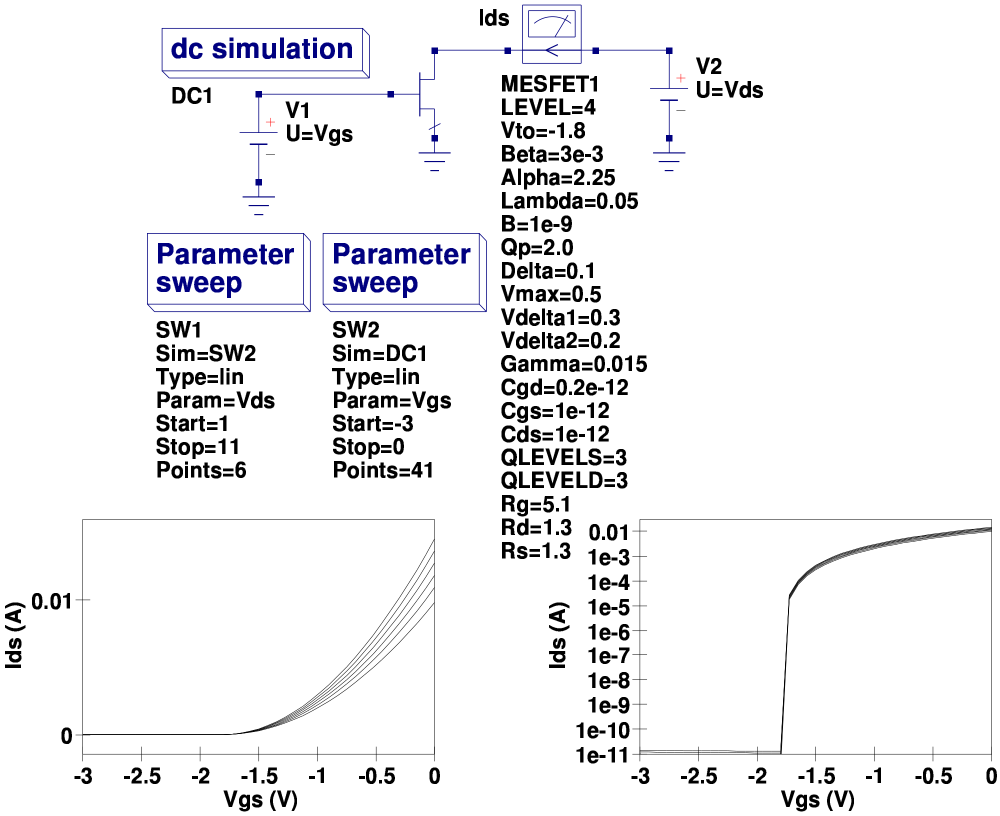


Figure 12: TOM1 LEVEL 4 DC test circuit and Ids-Vgs characteristics

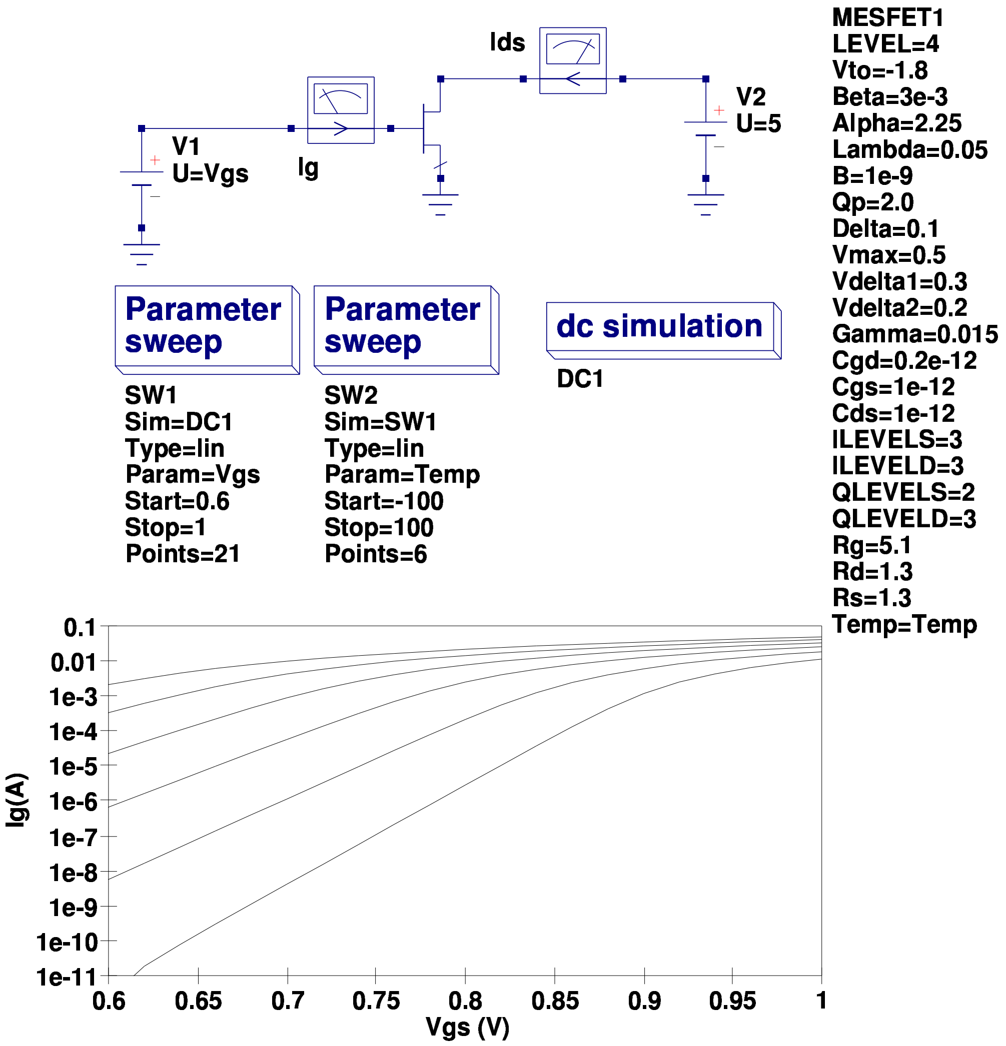


Figure 13: TOM1 LEVEL 4 DC test circuit and Ig-Vgs characteristics

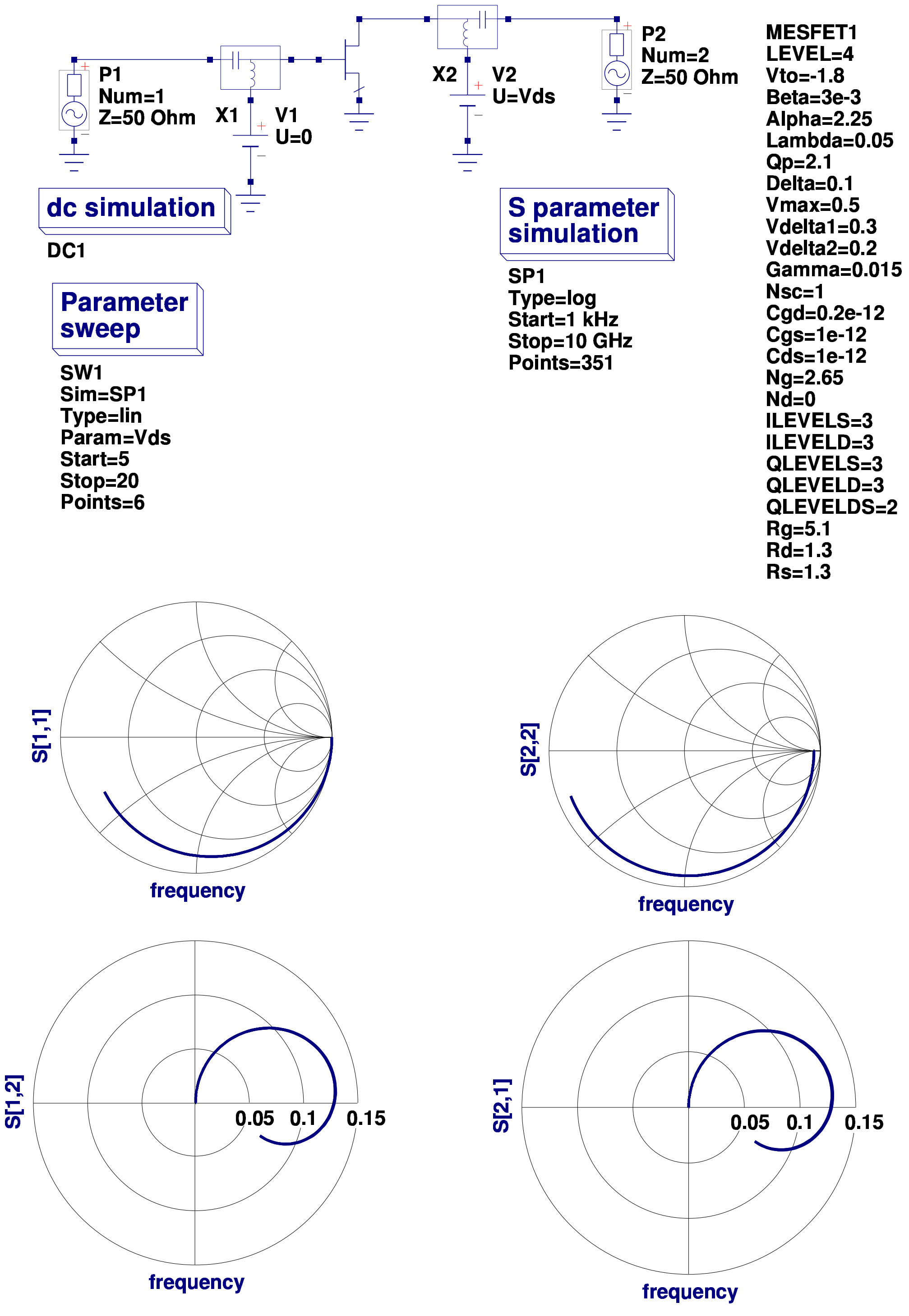


Figure 14: TOM1 LEVEL 4 S parameter test circuit and characteristics

TriQuint Semiconductor TOM 2 model: LEVEL = 5

```
if $(V(b1) - Vto\_T2) > 0$
    begin
        $Nst = Ng + Nd \cdot V(b3)$    (40)
        if $(Nst < 1.0) Nst = 1.0$
        $Vst = Nst \cdot Vt\_T2$    (41)
        $Vg = Qp \cdot Vst \cdot ln\left(exp\left\{\frac{V(b1) - Vto\_T2 + Gamma\_T2 \cdot V(b3)}{Qp \cdot Vst}\right\} + 1\right)$    (42)
        $Al = Alpha\_T2 \cdot V(b3)$    (43)
        $Fd = \frac{Al}{\sqrt{1 + Al \cdot Al}}$    (44)
        $Ids1 = Beta\_T2 \cdot Vg^{Qp} \cdot Fd$    (45)
        $Ids = Ids1 \cdot \frac{1 + Lambda \cdot V(b3)}{1 + Delta \cdot V(b3) \cdot Ids1}$    (46)
    end
else $Ids = 0$
```

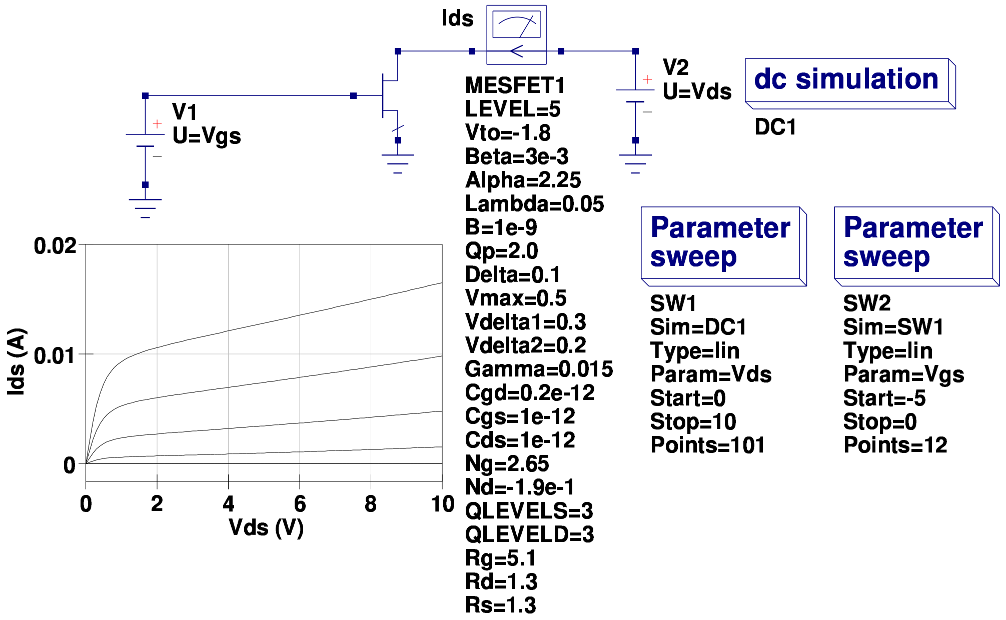


Figure 15: TOM2 LEVEL 5 DC test circuit and Ids-Vds characteristics

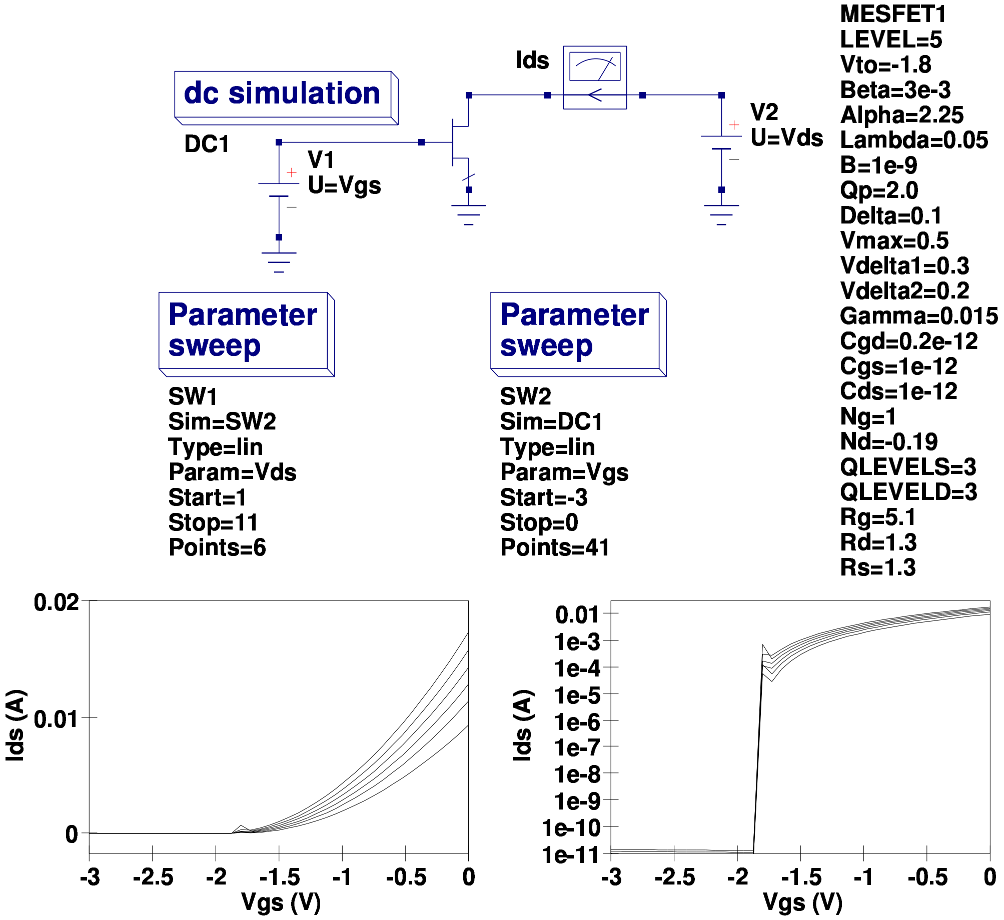


Figure 16: TOM2 LEVEL 5 DC test circuit and Ids-Vgs characteristics

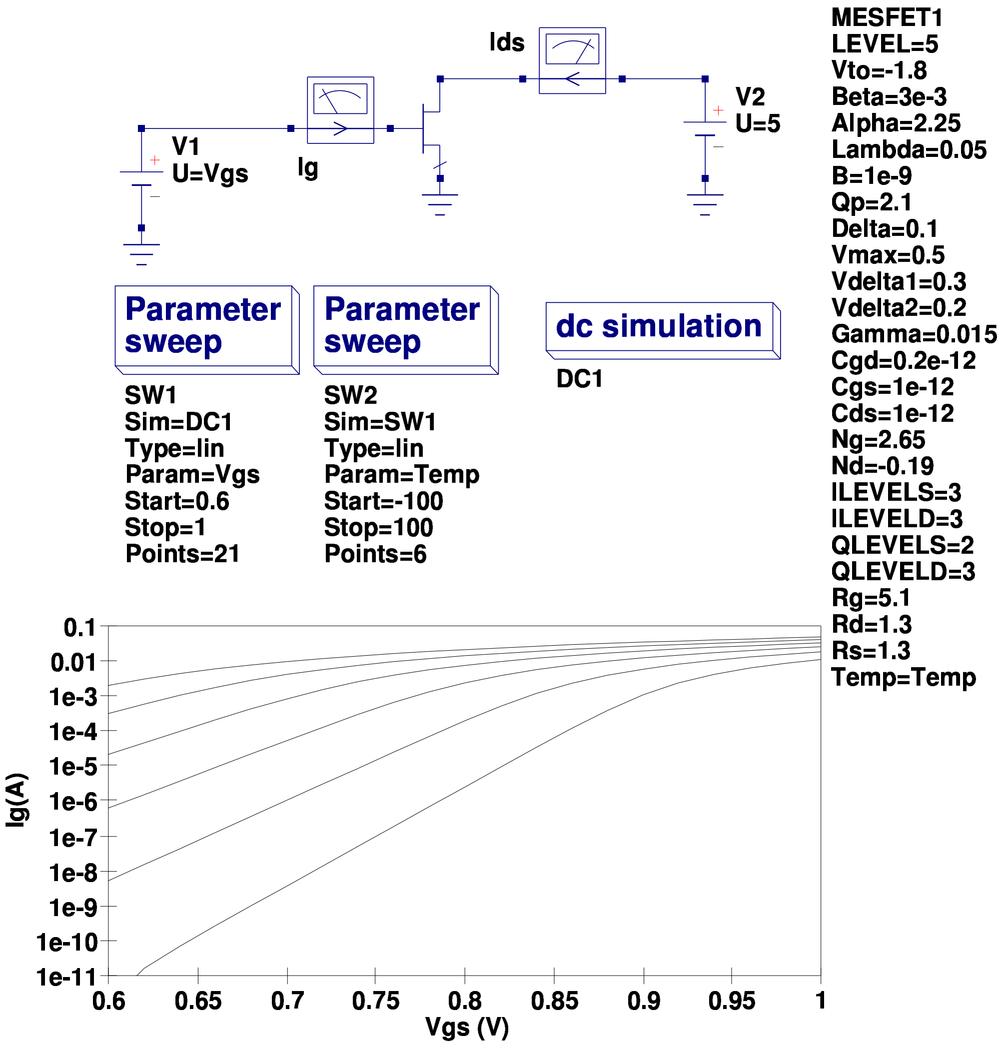


Figure 17: TOM2 LEVEL 5 DC test circuit and Ig-Vgs characteristics

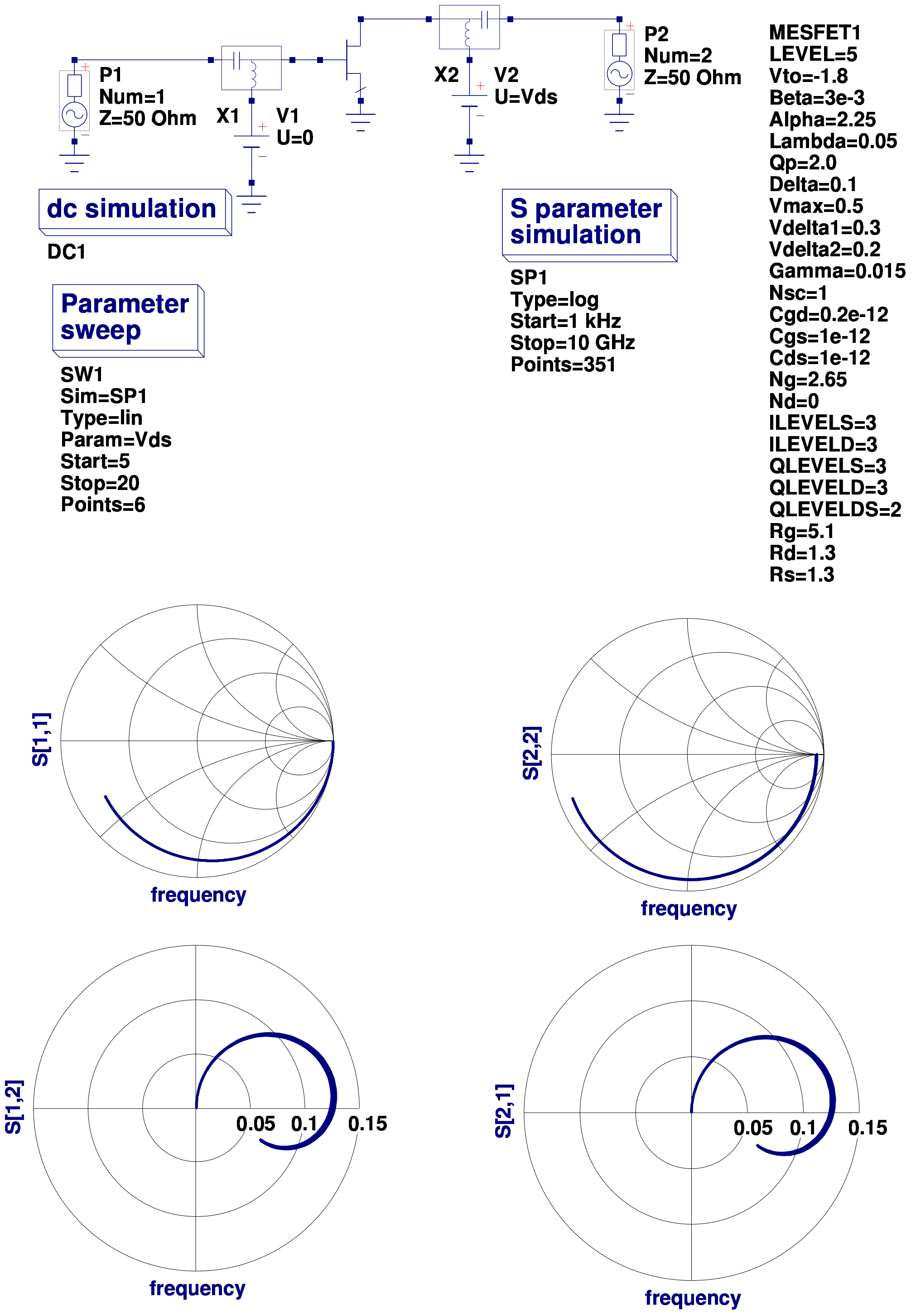


Figure 18: TOM2 LEVEL 5 S parameter test circuit and characteristics

Temperature scaling relations

```
T1=Tnom+273.15;
T2=Temp+273.15;
Tr=T2/T1;
con1=pow(Tr, 1.5);
Rg_T2=Rg*(1+Rgtc*(T2-T1));
Rd_T2=Rd*(1+Rdtc*(T2-T1));
Rs_T2=Rs*(1+Rstc*(T2-T1));
Beta_T2=Area*Beta*pow(1.01, Betatc*(T2-T1));
Vt_T2=$vt;
Eg_T1=Eg-7.02e-4*T1*T1/(1108+T1);
Eg_T2=Eg-7.02e-4*T2*T2/(1108+T2);
Vbi_T2=(Tr*Vbi)-(2*Vt_T2*ln(con1)) - ( Tr*Eg_T1-Eg_T2);
Is_T2=Area*Is*pow( Tr, (Xti/N))*limexp(-(‘P_Q*Eg_T1)*(1-Tr)/(‘P_K*T2));
Cgs_T2=Area*Cgs*(1+M*(400e-6*(T2-T1)-(Vbi_T2-Vbi)/Vbi));
Cgd_T2=Area*Cgd*(1+M*(400e-6*(T2-T1)-(Vbi_T2-Vbi)/Vbi));
Vto_T2=Vto+Vtotc*(T2-T1);
Gamma_T2=Gamma*(1+Gammatc*(T2-T1));
Alpha_T2=Alpha*( pow( 1.01, Alphatc*(T2-T1)));
```

MESFET noise

Main components

- Thermal noise: generated by resistors Rg, Rd and Rs.
- Channel noise: 1. Linear region: essentially thermal noise; 2. Saturation region: diffusion noise.
- Gate noise: Mainly channel noise induced in the gate (via the channel to gate capacitance) The resulting noise is amplified by the MESFET. The capacitive coupling causes the gate noise to have a power spectral density proportional to frequency.
- Flicker noise: Due to random carrier generation-recombination in the lattice imperfections or contaminating impurities. Flicker noise power has a $\frac{1}{f^n}$ behavior, with $n \approx 1$.

A typical plot of GaAs MESFET Ids noise current is shown in Fig. 19, where the

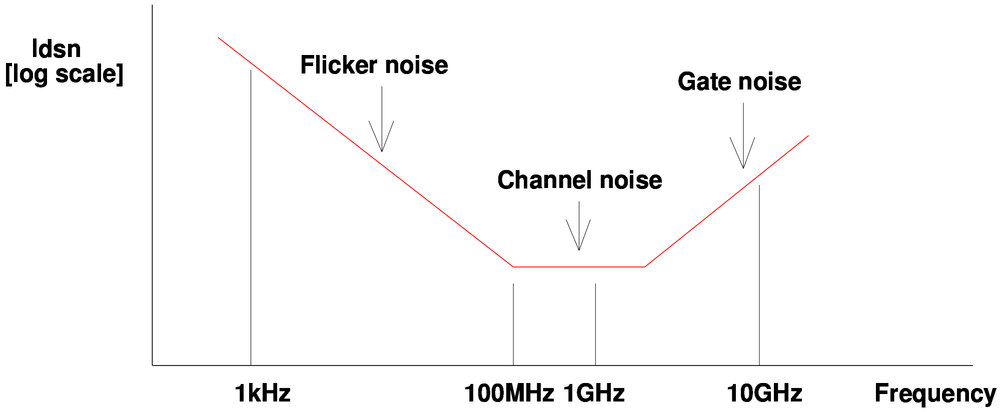


Figure 19: Typical GaAS MESFET Ids noise characteristic

device drain to source noise current is given by

$$Idsn = \text{channel-thermal-noise-current} + \text{flicker-noise-current} \tag{47}$$

To a first approximation:

- Channel-thermal-noise-current[7] $= \sqrt{\frac{8 \cdot K \cdot T}{3} \cdot gm \cdot \left\{ \frac{1+\alpha+\alpha^2}{1+\alpha} \right\} \cdot Gdsnoi}$

  Where $gm = \frac{\partial Ids}{\partial Vgs}$,

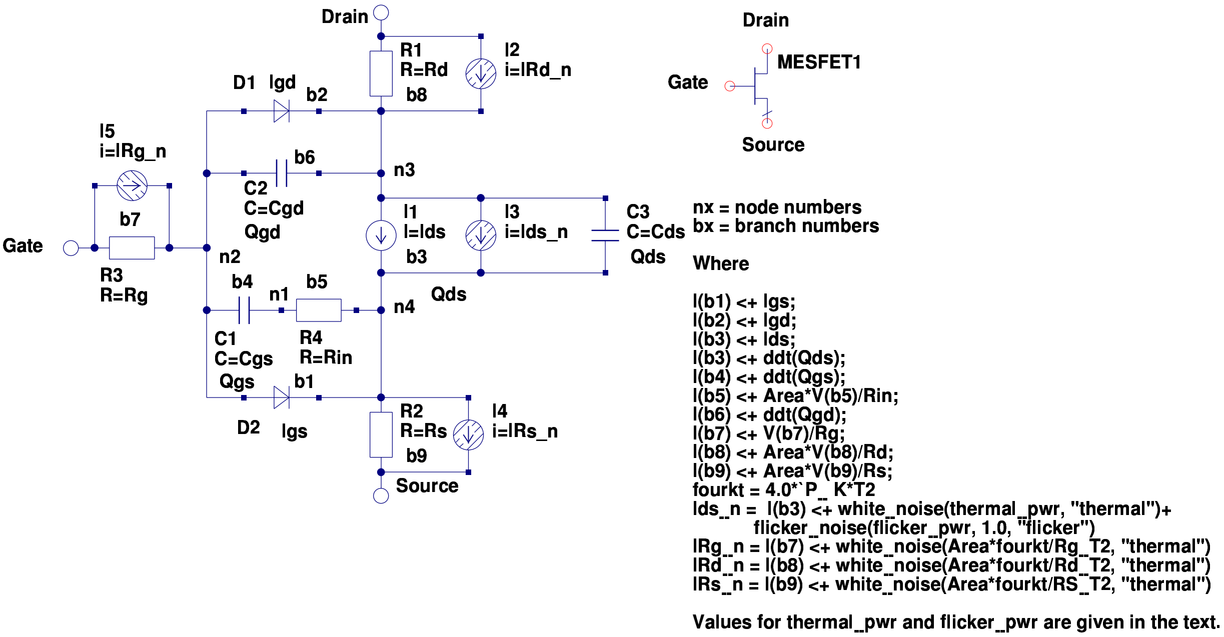
  and $\alpha = 1 - \frac{Vds}{Vgs - Vto}$, when $Vds < \frac{3}{Alpha}$ – Linear region of operation

  Or $\quad \alpha = 0$, when $Vds >= \frac{3}{Alpha}$ – Saturation region of operation

- flicker-noise-current $= \sqrt{\frac{Kf \cdot Ids^{Af}}{f}}$

- Resister thermal noise equations $IRgn = \sqrt{\frac{4 \cdot K \cdot T}{Rg}}$, $IRdn = \sqrt{\frac{4 \cdot K \cdot T}{Rd}}$,

  and $IRsn = \sqrt{\frac{4 \cdot K \cdot T}{Rs}}$



```
nx = node numbers
bx = branch numbers

Where

I(b1) <+ Igs;
I(b2) <+ Igd;
I(b3) <+ Ids;
I(b3) <+ ddt(Qds);
I(b4) <+ ddt(Qgs);
I(b5) <+ Area*V(b5)/Rin;
I(b6) <+ ddt(Qgd);
I(b7) <+ V(b7)/Rg;
I(b8) <+ Area*V(b8)/Rd;
I(b9) <+ Area*V(b9)/Rs;
fourkt = 4.0*`P_ K*T2
Ids_n =  I(b3) <+ white_noise(thermal_pwr, "thermal")+
          flicker_noise(flicker_pwr, 1.0, "flicker")
IRg_n = I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal")
IRd_n = I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal")
IRs_n = I(b9) <+ white_noise(Area*fourkt/RS_T2, "thermal")

Values for thermal_pwr and flicker_pwr are given in the text.
```

Figure 20: Typical GaAS MESFET equivalent circuit illustrating noise current components

MESFET equivalent circuit with noise current components

Curtice hyperbolic tangent model: LEVEL = 1 or 2: Noise equations

1. Verilog-A equations

```
fourkt=4.0*‘P_K*T2;
gm=2*Beta_T2*(V(b1)-Vto_T2)*(1+Lambda*V(b3))*tanh(Alpha_T2*V(b3));
   if ( V(b3) < 3/Alpha ) begin  An=1-V(b3)/(V(b1)-Vto_T2);
    thermal_pwr= (8*‘P_K*T2*gm/3)*((1+An+An*An)/(1+An))*Gdsnoi;
   end
   else
    thermal_pwr=(8*‘P_K*T2*gm/3)*Gdsnoi;
    I(b3)<+white_noise(thermal_pwr,"thermal"); flicker_pwr = Kf*pow(Ids,Af);
    I(b3)<+flicker_noise(flicker_pwr,1.0,"flicker");
   end
I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");
I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal");
```

---

[7] Tsivids and Yanis, Operation and modeling of the MOS transistor, McGraw-HIll 1987, p340

```
I(b9) <+ white_noise(Area*fourkt/Rs_T2, "thermal");
```

2. Typical noise simulation results

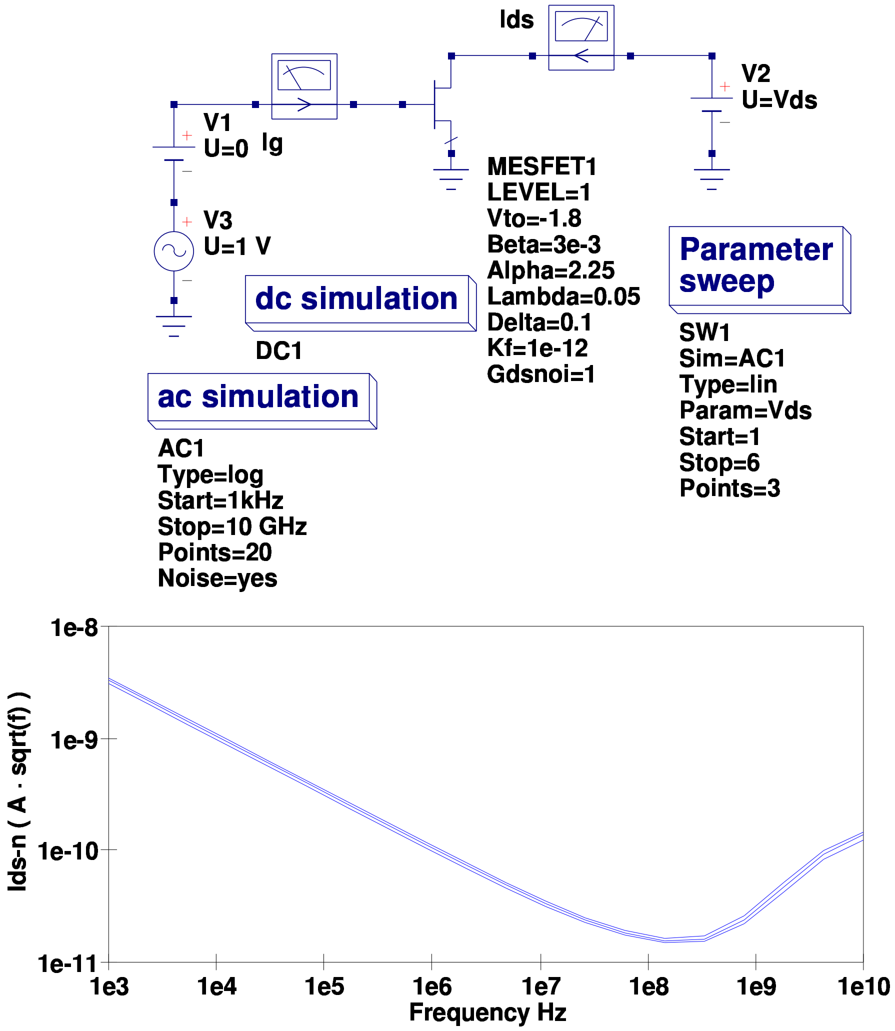


Figure 21: Typical LEVEL 1 (or 2) GaAS MESFET Ids noise characteristic

Statz *et. al.* (Raytheon) model: LEVEL = 3: Noise equations

1. Verilog-A equations

```
if ( V(b3) < 3/Alpha )begin
```

```
H1=(1-(1-(Alpha*V(b3))/3))/(1+B*(V(b1)-Vto_T2));
gm=2*Beta_T2*(V(b1)-Vto_T2)*(1+Lambda*V(b3))*H1+(Beta_T2*
   (1+Lambda*V(b3))*pow((V(b1)-Vto_T2),2))*B*H1/(1+B*(V(b1)-Vto_T2));
An=1-V(b3)/(V(b1)-Vto_T2);
thermal_pwr= (8*‘P_K*T2*gm/3)*((1+An+An*An)/(1+An))*Gdsnoi;
end
else begin
gm=2*Beta_T2*(V(b1)-Vto_T2)*(1+Lambda*V(b3))/(1+B*(V(b1)-Vto_T2))+
(Beta_T2*(1+Lambda*V(b3))*pow((V(b1)-Vto_T2),2))
*B/pow( (1+B*(V(b1)-Vto_T2)),2);
thermal_pwr=(8*‘P_K*T2*gm/3)*Gdsnoi;
end
I(b3) <+ white_noise(thermal_pwr, "thermal");
flicker_pwr = Kf*pow(Ids,Af);
I(b3) <+ flicker_noise(flicker_pwr,1.0, "flicker");
I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");
I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal");
I(b9) <+ white_noise(Area*fourkt/Rs_T2, "thermal");
```

2. Typical noise simulation results

TriQuint Semiconductor TOM 1 model: LEVEL = 4: Noise equations

1. Verilog-A equations

```
if ( V(b3) < 3/Alpha )begin
Ids1=(Beta_T2*pow( (V(b1)-Vto_T2), Qp) )*(1-pow( (1-Alpha*V(b3)/3), 3));
gm1=Qp*Beta_T2*pow( V(b1)-Vto_T2, Qp-1)*(1-(1-pow(Alpha*V(b3)/3, 3)));
gm=(gm1*(1+Lambda*V(b3))/(1+Delta*V(b1)*Ids1))*(1+(Delta*V(b3)*Ids1)/
   (1+Delta*V(b3)*Ids1));
        An=1-V(b3)/(V(b1)-Vto_T2);
thermal_pwr= (8*‘P_K*T2*gm/3)*((1+An+An*An)/(1+An))*Gdsnoi;
end
else begin
Ids1=(Beta_T2*pow( (V(b1)-Vto_T2), Qp) );
gm1=Qp*Beta_T2*pow( V(b1)-Vto_T2, Qp-1);
gm=(gm1*(1+Lambda*V(b3))/(1+Delta*V(b1)*Ids1))*(1+(Delta*V(b3)*Ids1)/
   (1+Delta*V(b3)*Ids1));
        thermal_pwr=(8*‘P_K*T2*gm/3)*Gdsnoi;
end
```

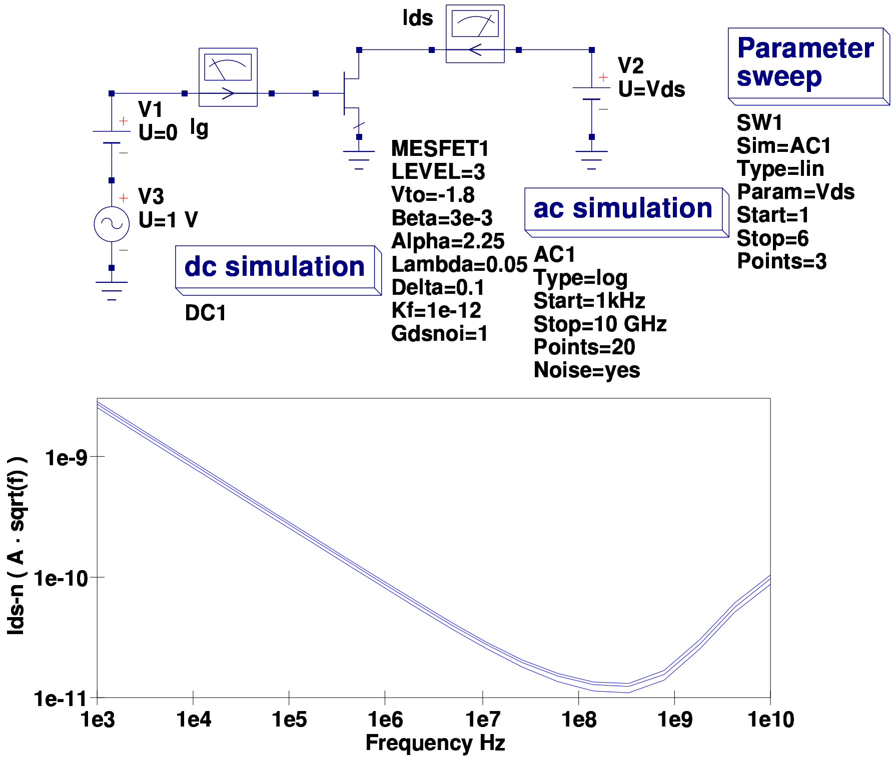


Figure 22: Typical LEVEL 3 GaAS MESFET Ids noise characteristic

```
I(b3) <+ white_noise(thermal_pwr, "thermal");
flicker_pwr = Kf*pow(Ids,Af);
I(b3) <+ flicker_noise(flicker_pwr,1.0, "flicker");
I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");
I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal");
I(b9) <+ white_noise(Area*fourkt/Rs_T2, "thermal");
```

2. Typical noise simulation results

TriQuint Semiconductor TOM 2 model: LEVEL = 5

1. Verilog-A equations

```
if ( V(b3) < 3/Alpha )begin
Nst=Ng+Nd*V(b3);
if ( Nst < 1.0) Nst=1.0;
 Vst=Nst*Vt_T2;
 Vg=Qp*Vst*ln( exp( (V(b1)-Vto_T2+Gamma_T2*V(b3)) / (Qp*Vst) ) + 1);
```

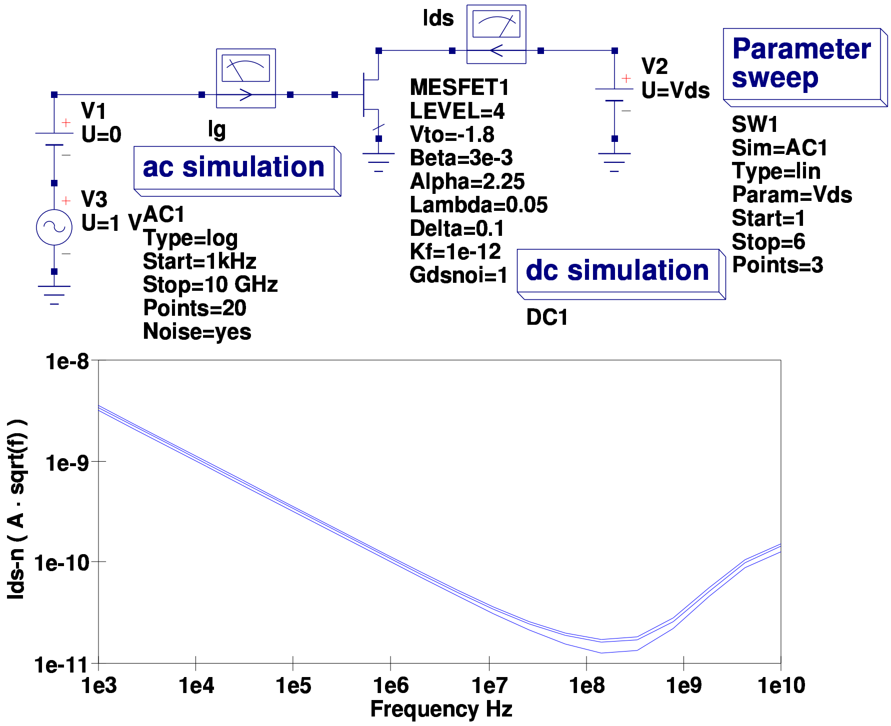


Figure 23: Typical LEVEL 4 GaAS MESFET Ids noise characteristic

```
 Al= Alpha_T2*V(b3); Fd=Al/sqrt( 1.0+(Al*Al) );
 Ids1=Beta_T2*pow( Vg, Qp)*Fd;
 gm1=(Ids1/Vg)*Qp/(exp(-((V(b1)-Vto_T2+Delta*V(b3))/(Qp*Vst)))+1);
 gm=gm1/pow( (1+Delta*V(b3)*Ids1),2);
         An=1-V(b3)/(V(b1)-Vto_T2);
   thermal_pwr= (8*‘P_K*T2*gm/3)*((1+An+An*An)/(1+An))*Gdsnoi;
end
else begin
 Nst=Ng+Nd*V(b3); if ( Nst < 1.0) Nst=1.0;
 Vst=Nst*Vt_T2;
 Vg=Qp*Vst*ln( exp( (V(b1)-Vto_T2+Gamma_T2*V(b3)) / (Qp*Vst) ) + 1);
 Al= Alpha_T2*V(b3); Fd=Al/sqrt( 1.0+(Al*Al) );
 Ids1=Beta_T2*pow( Vg, Qp)*Fd;
 gm1=(Ids1/Vg)*Qp/(exp(-((V(b1)-Vto_T2+Delta*V(b3))/(Qp*Vst)))+1);
 gm=gm1/pow( (1+Delta*V(b3)*Ids1),2);
 thermal_pwr=(8*‘P_K*T2*gm/3)*Gdsnoi;
end
I(b3) <+ white_noise(thermal_pwr, "thermal");
```

```
flicker_pwr = Kf*pow(Ids,Af);
I(b3) <+ flicker_noise(flicker_pwr,1.0, "flicker");
I(b7) <+ white_noise(Area*fourkt/Rg_T2, "thermal");
I(b8) <+ white_noise(Area*fourkt/Rd_T2, "thermal");
I(b9) <+ white_noise(Area*fourkt/Rs_T2, "thermal");
```

2. Typical noise simulation results

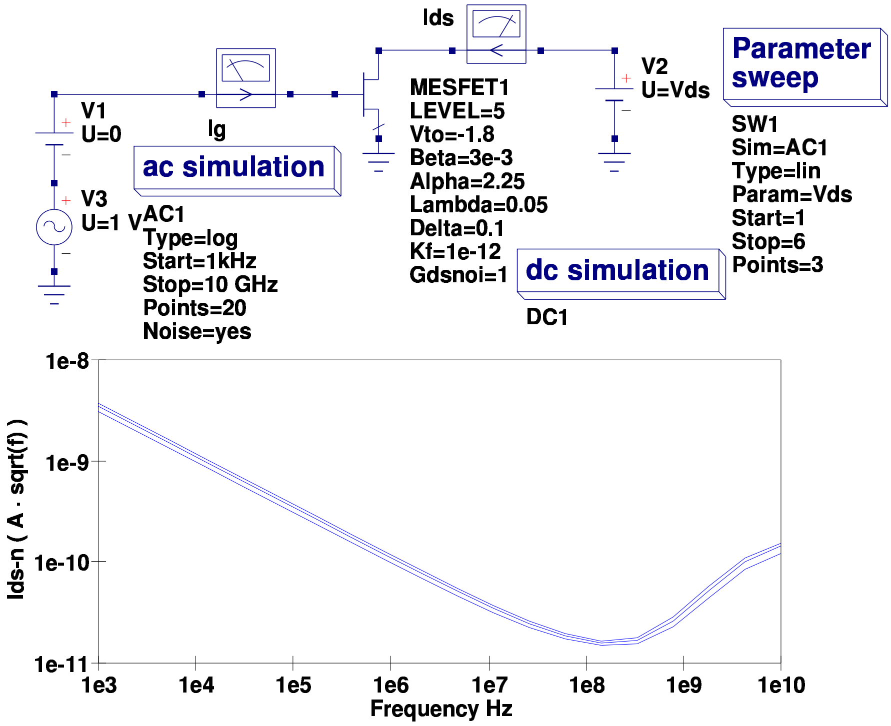


Figure 24: Typical LEVEL 5 GaAS MESFET Ids noise characteristic

Adding external passive components to the MESFET models

The Curtice model outlined in the first Qucs report on MESFETs included lead inductance in each of the device signal paths. These inductances were not included in the Verilog-A models described in this report, mainly to simplify the model code. If required they can be added as external components. The test circuit shown in Fig. 25 indicates how this can be done and illustrates the effect such components have on the Curtice S parameter characteristics.

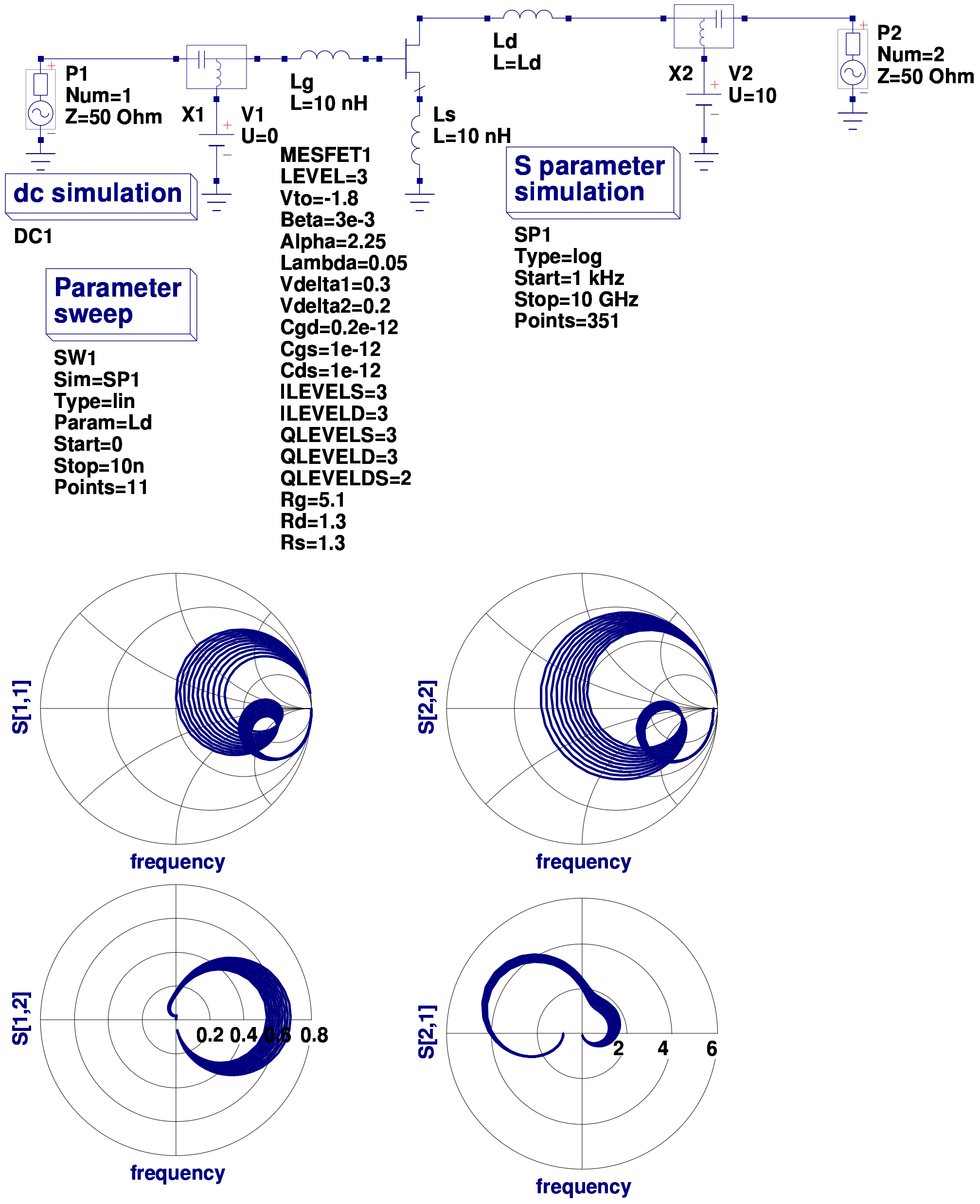


Figure 25: S parameter simulated characteristics for test circuit shown in Fig. 5 that has external inductance added

End note

MESFETs are important high frequency devices which have been missing from the range of active component models supplied with Qucs. While developing the models described in this report I have attempted to make them as flexible as possible so as to allow users the opportunity to select which model, or indeed the make-up of the components of a model, they would like to try for a specific simulation. The work described in this report is very much work in progress, mainly because there are a number of other published MESFET models that have not been included. My intention has simply been to provide a number of practical models which were not previously available to Qucs users. Also knowing that many Qucs users have an interest in high frequency circuit design and simulation, the work would be of direct relevance to making Qucs more "universal". The procedures employed for model development are another example of the work being undertaken by the Qucs team in response to Qucs being adopted by the wider modelling community as part of the Verilog-A compact device standardization project. Overall the simulation results from the models described here show a high degree of consistency from DC to the high frequency S parameter domain. The noise results are particularly interesting as they are based on mix of available theories and extensions introduced especially for Qucs. Some readers will probably have spotted one area where there appears to be differences in the simulation results from the different models; look at the S[1,2] and S[2,1] characterstics for each model. Here there are noticeable difference which are possibly due to the lack of symmetry in some of the model charge equations? MESFET modelling is a complex subject, suggesting that there are likely to be errors /bugs in the models. If you find an error/bug please inform the Qucs development team so that we can correct problems as they are found. In the future, particularly if the response to this group of models is positive, I will attempt to add more MESFET models to Qucs. Once again a special thanks to Stefan Jahn for all his help and encouragement over the period that I have been developing the Qucs MESFET models and writing the report which outlines their physical and mathematical fundamentals.